

# Operating Systems

## Lecture 13: TLB + Advanced Paging

Nipun Batra

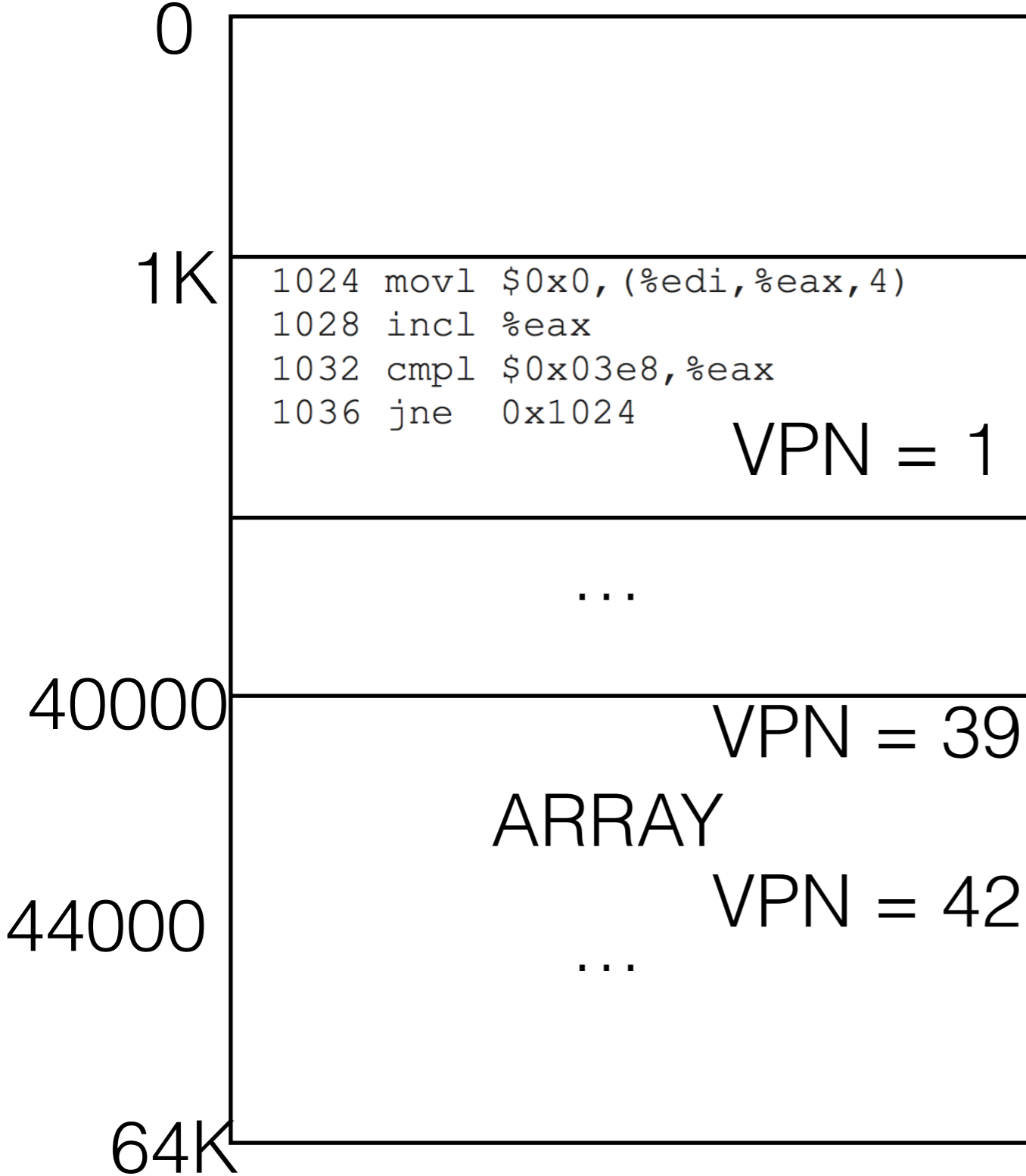
Aug 30, 2018

# Revision

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VA

PA

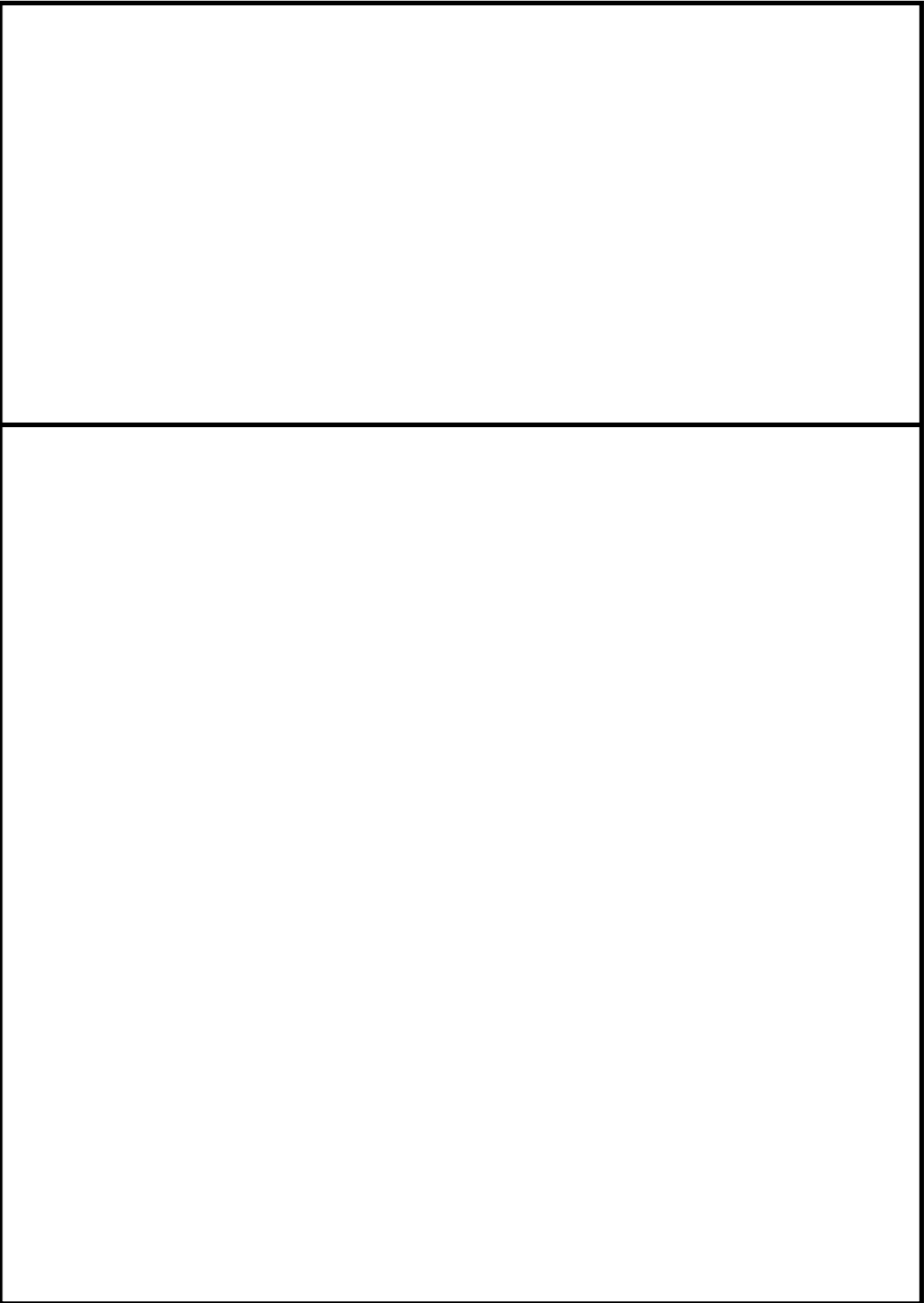
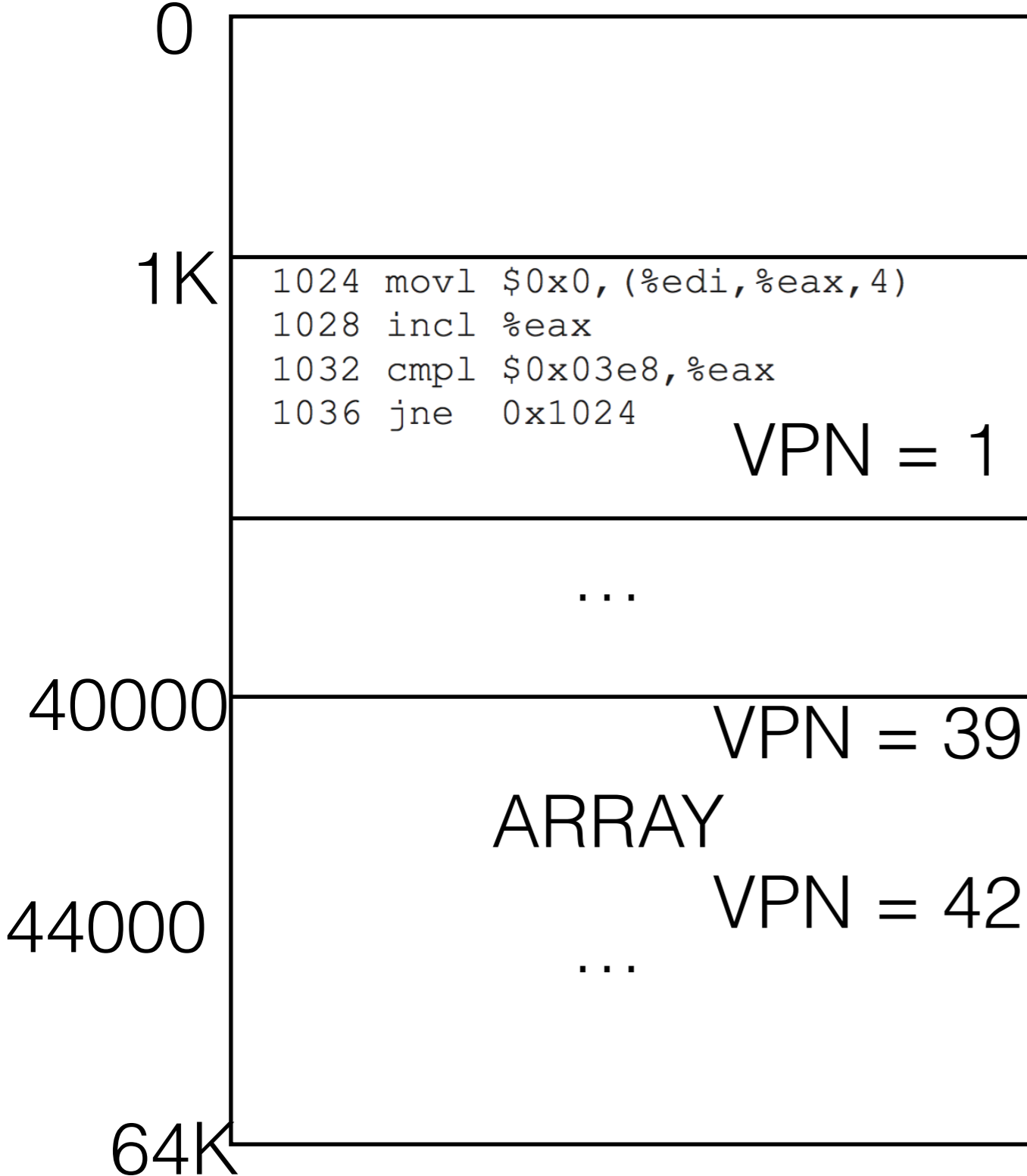


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PA

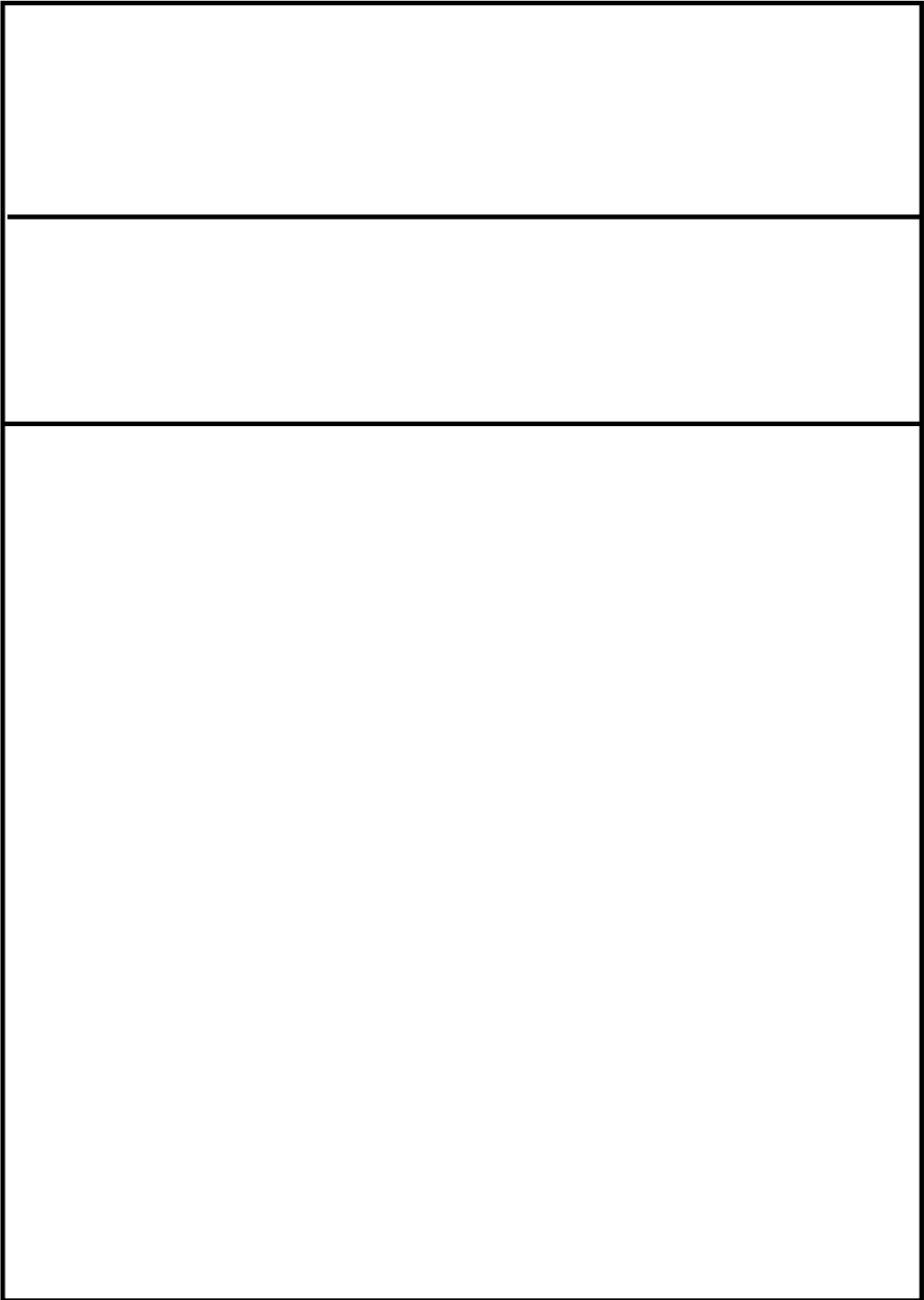
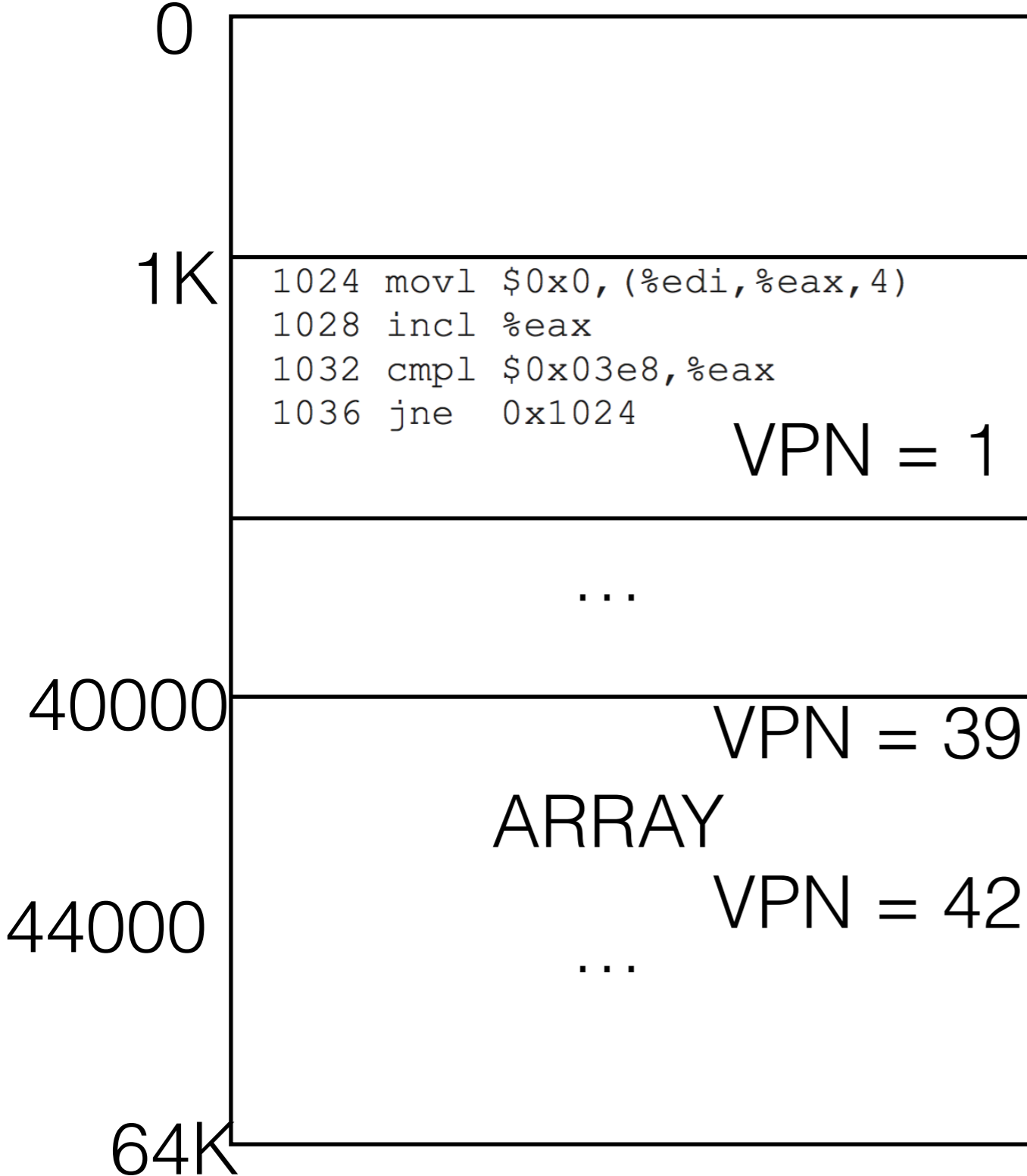


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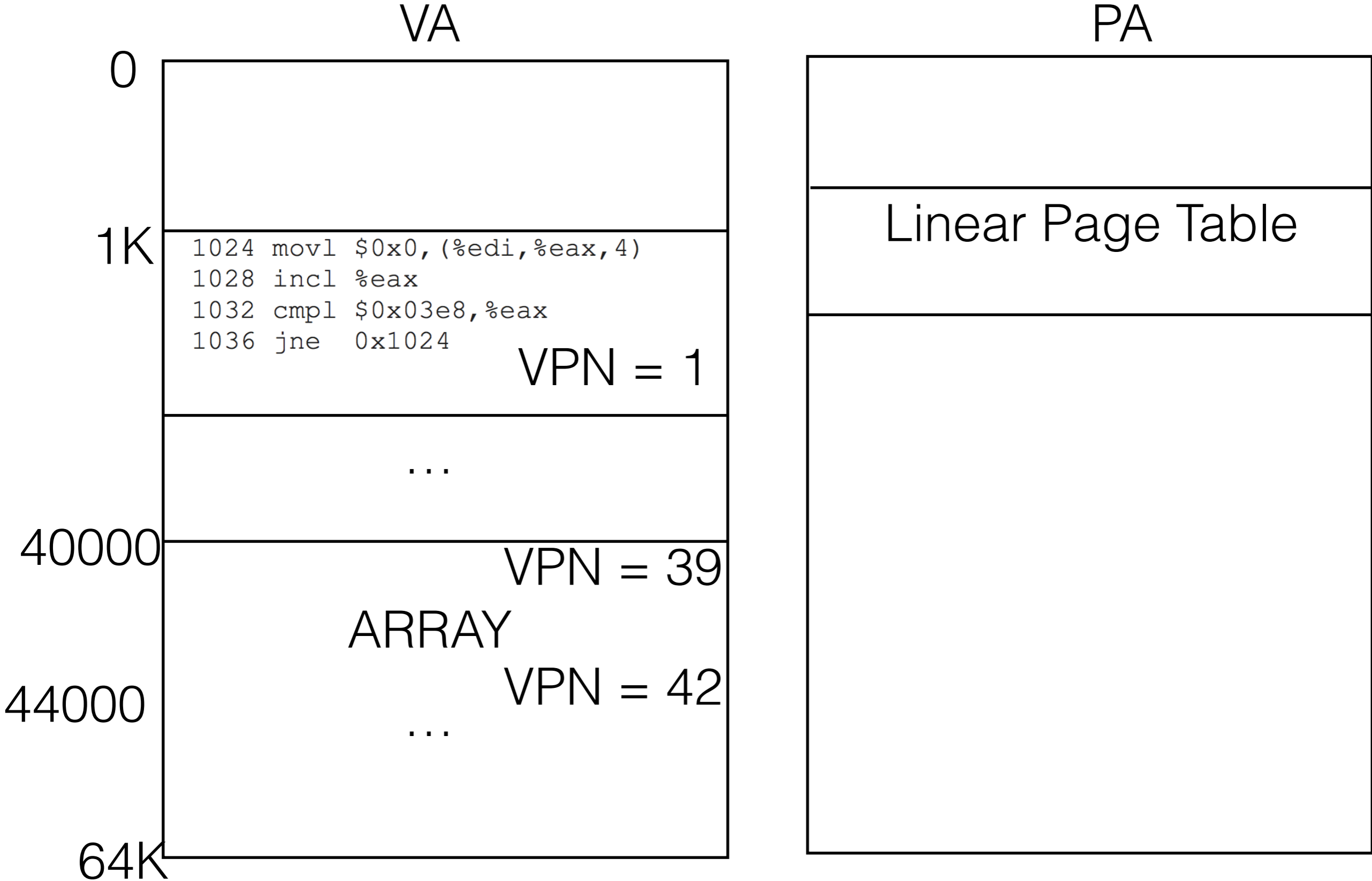
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VA

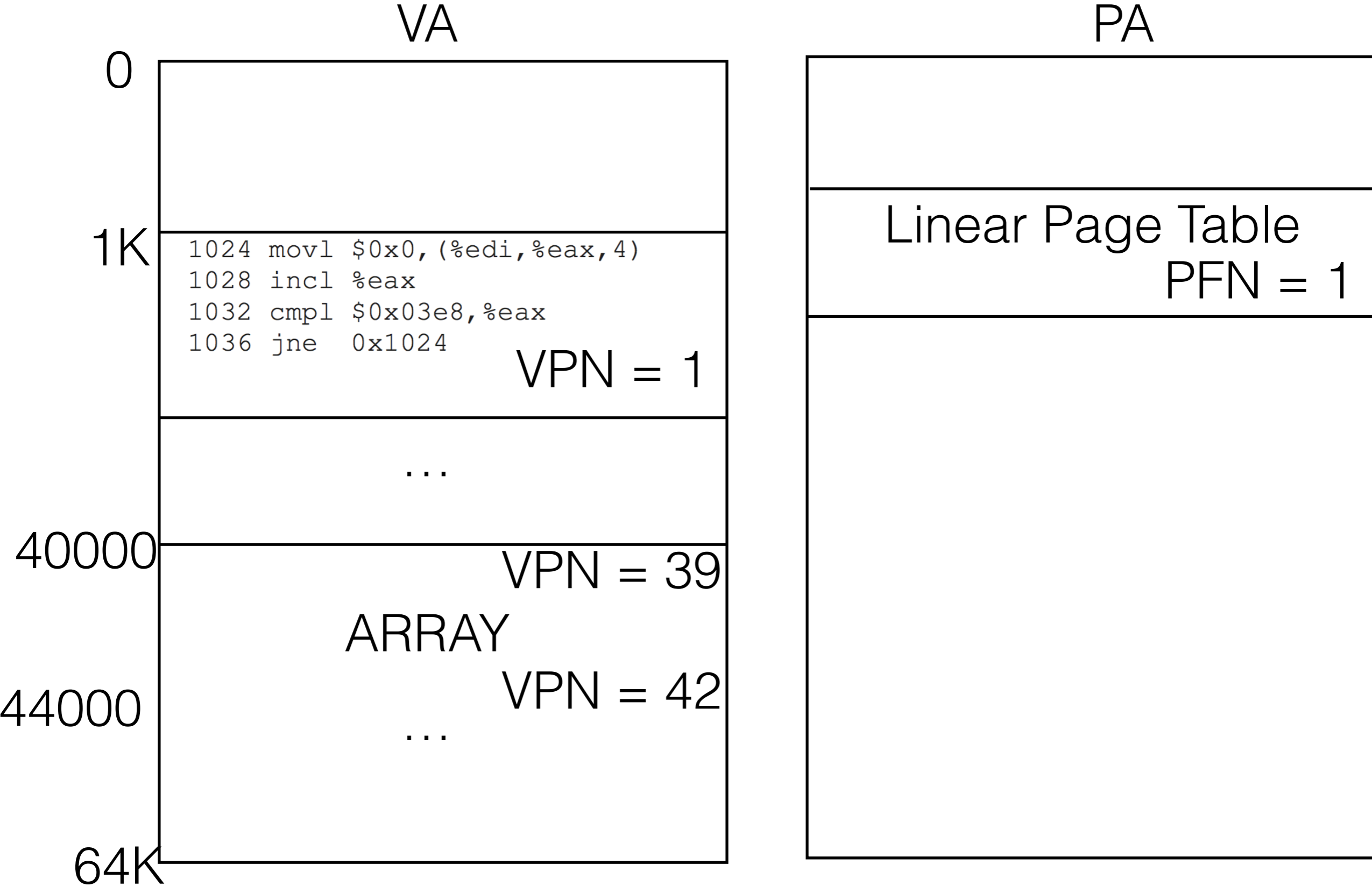
PA



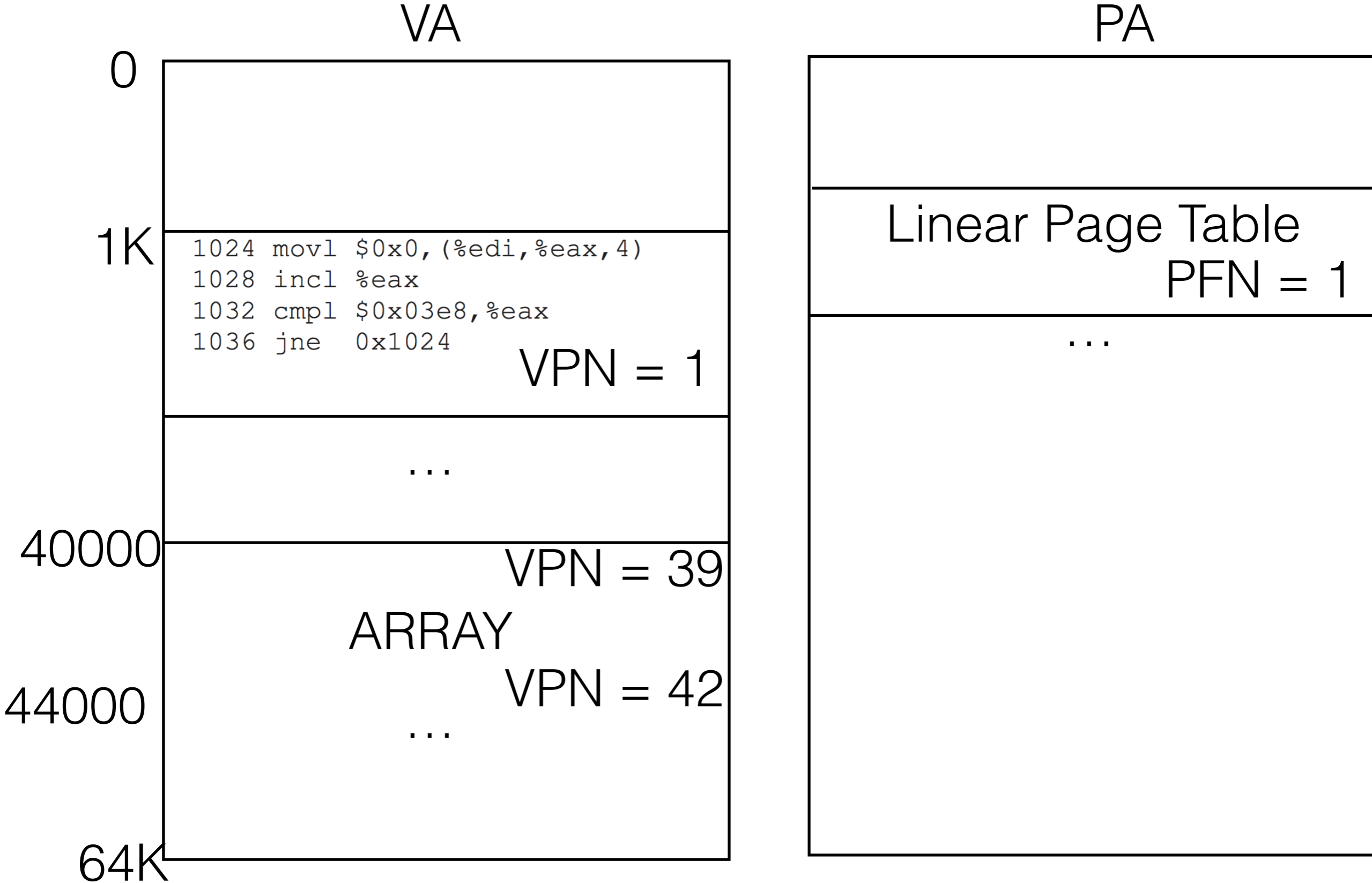
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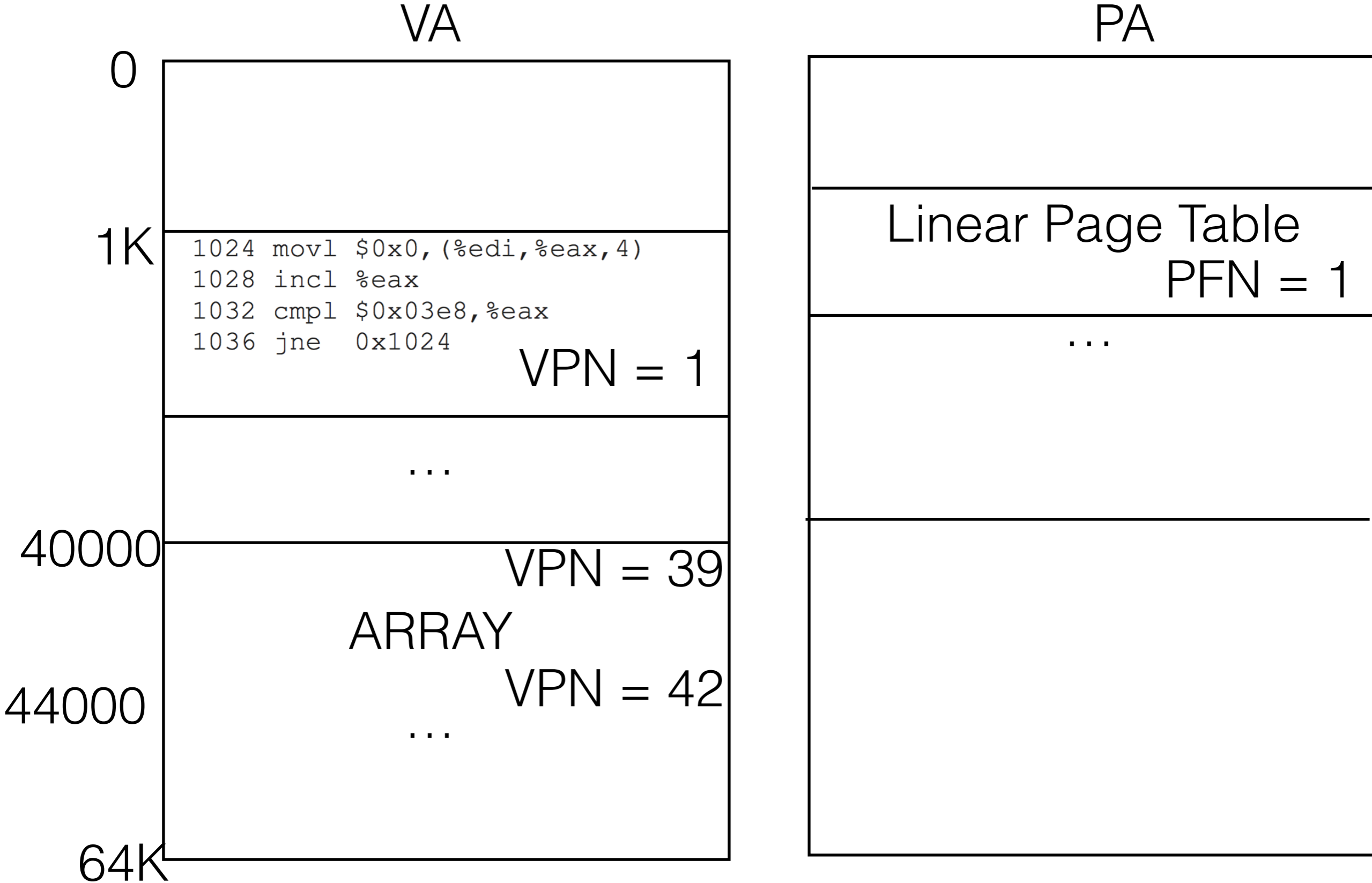


# Revision



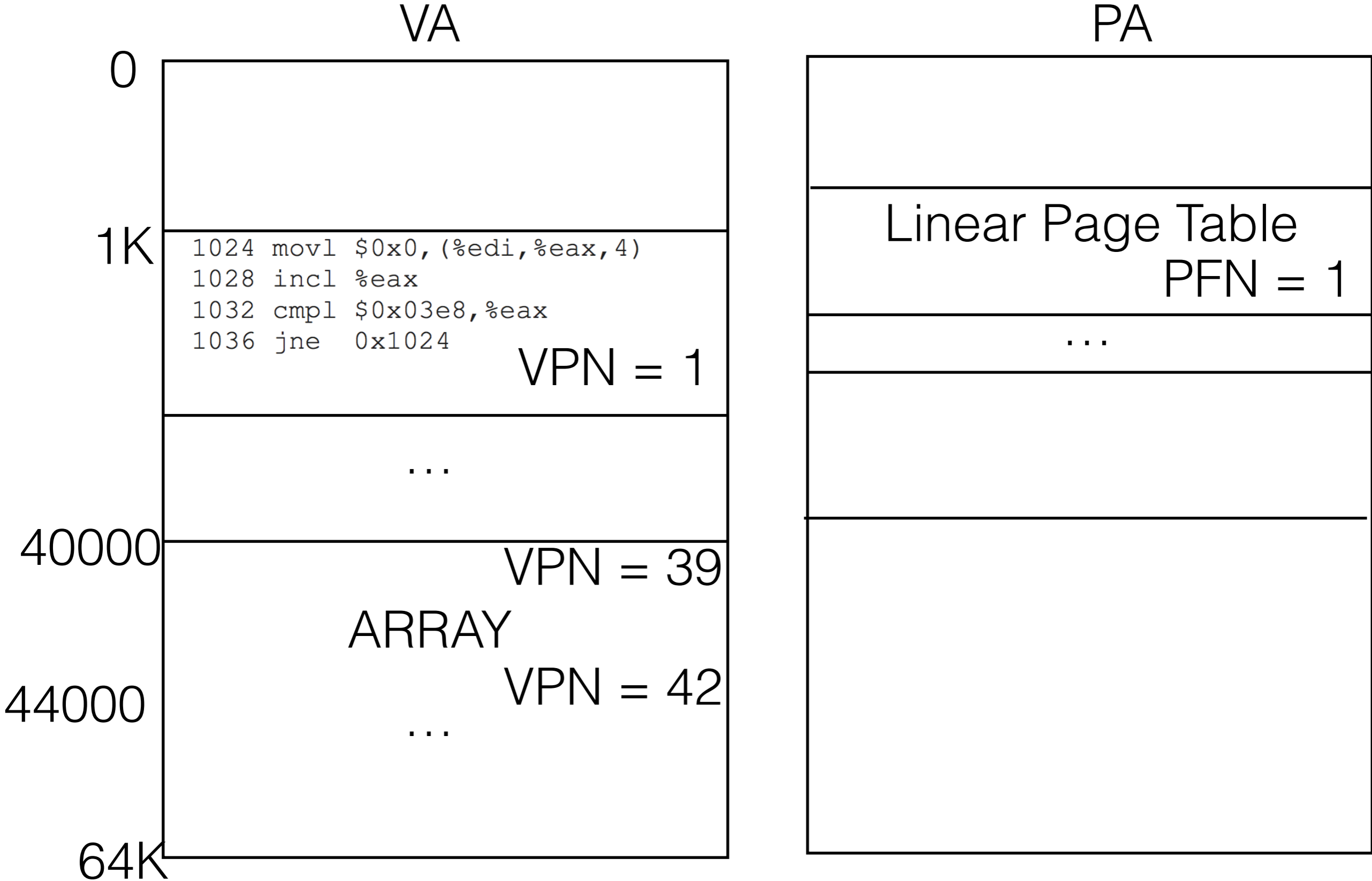
# Revision

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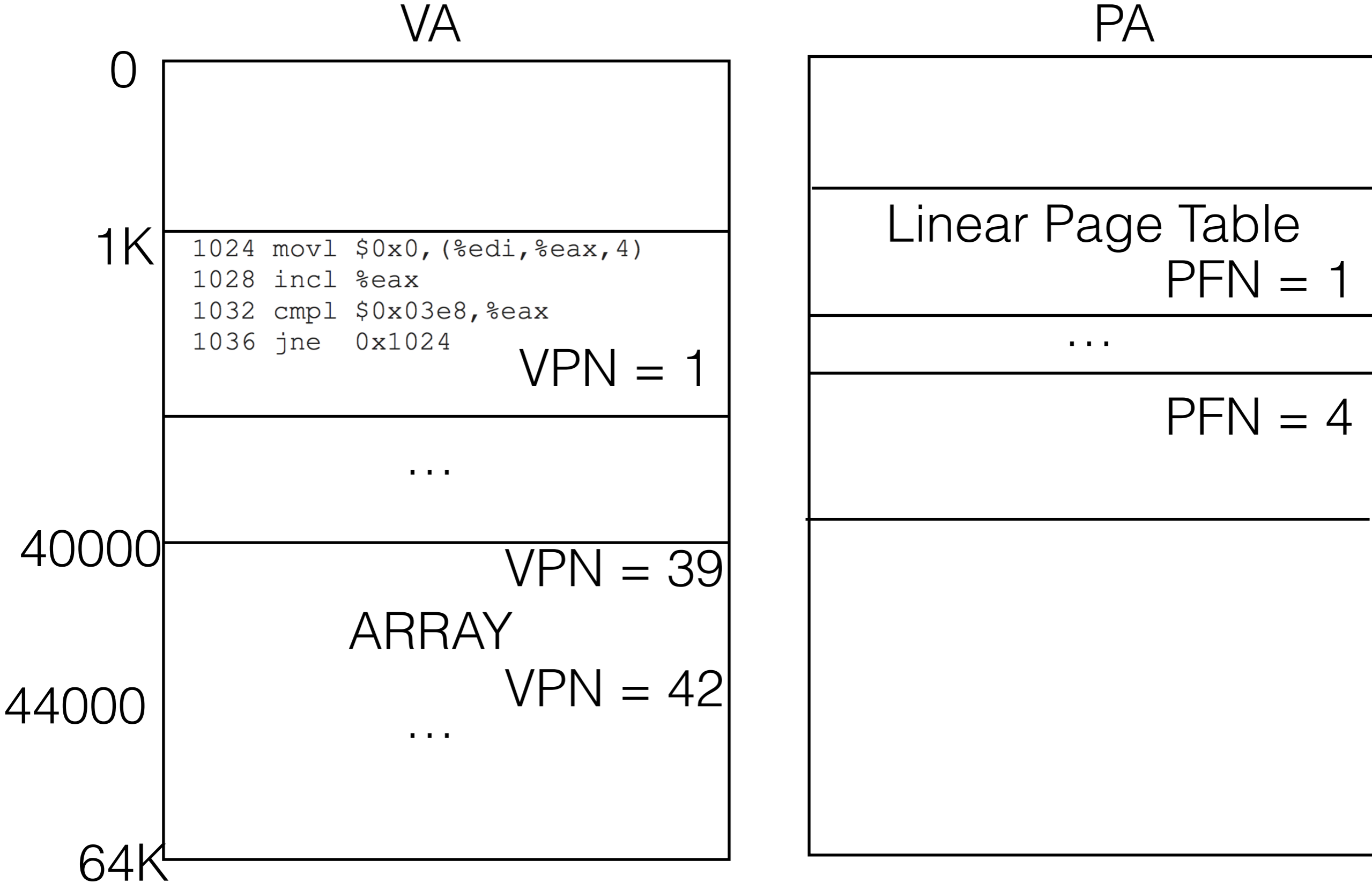




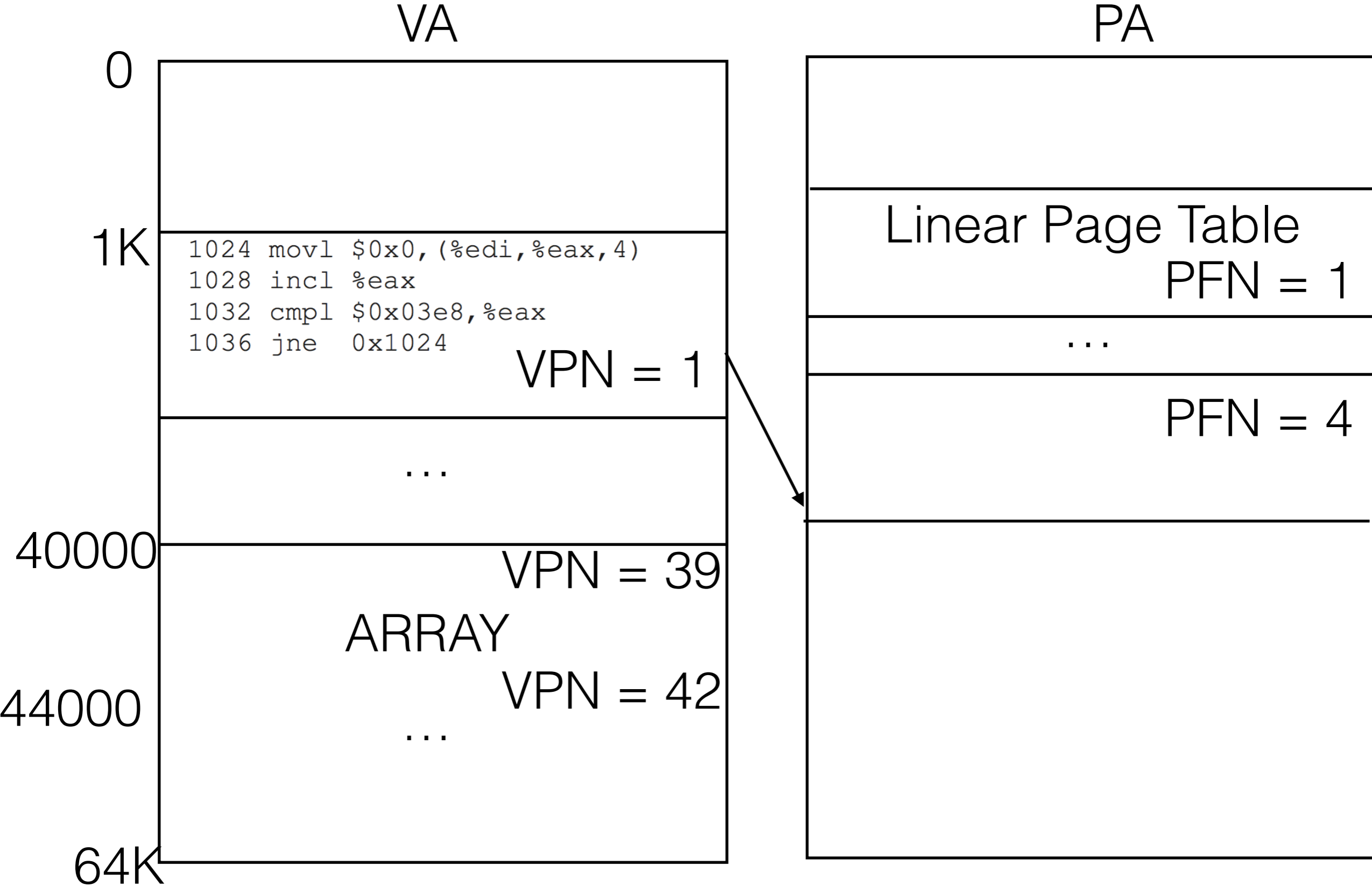
# Revision



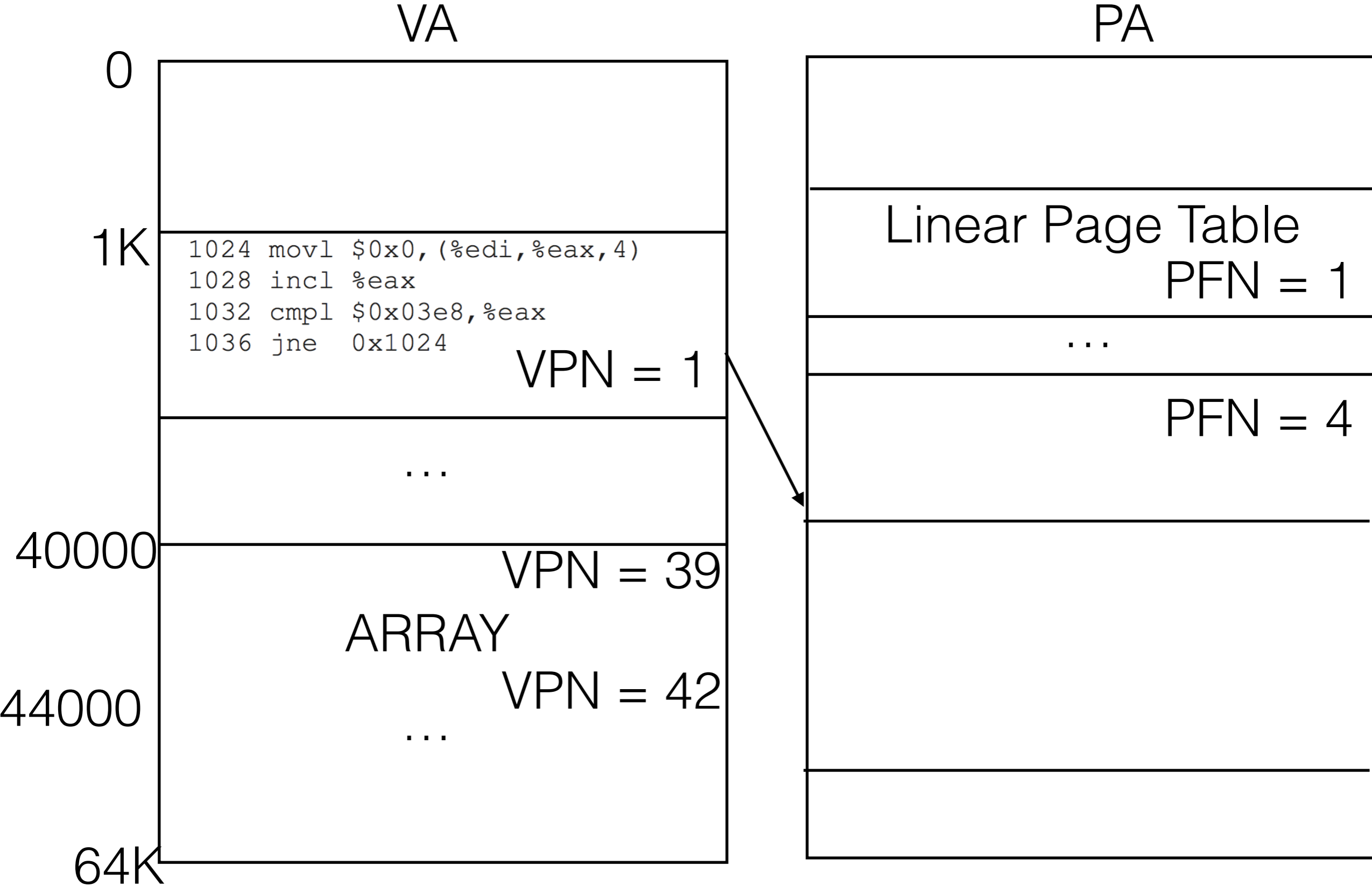
# Revision



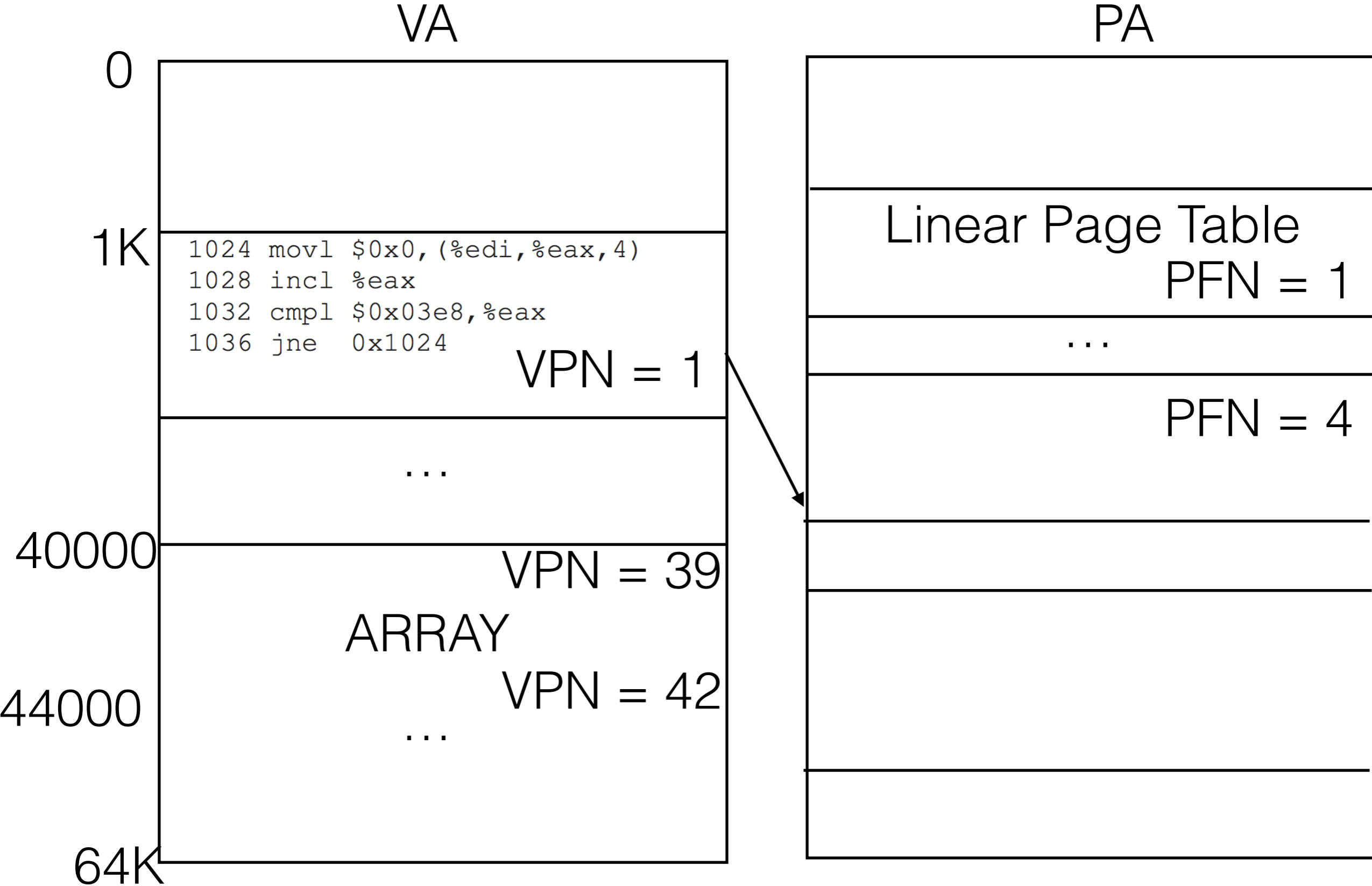
# Revision



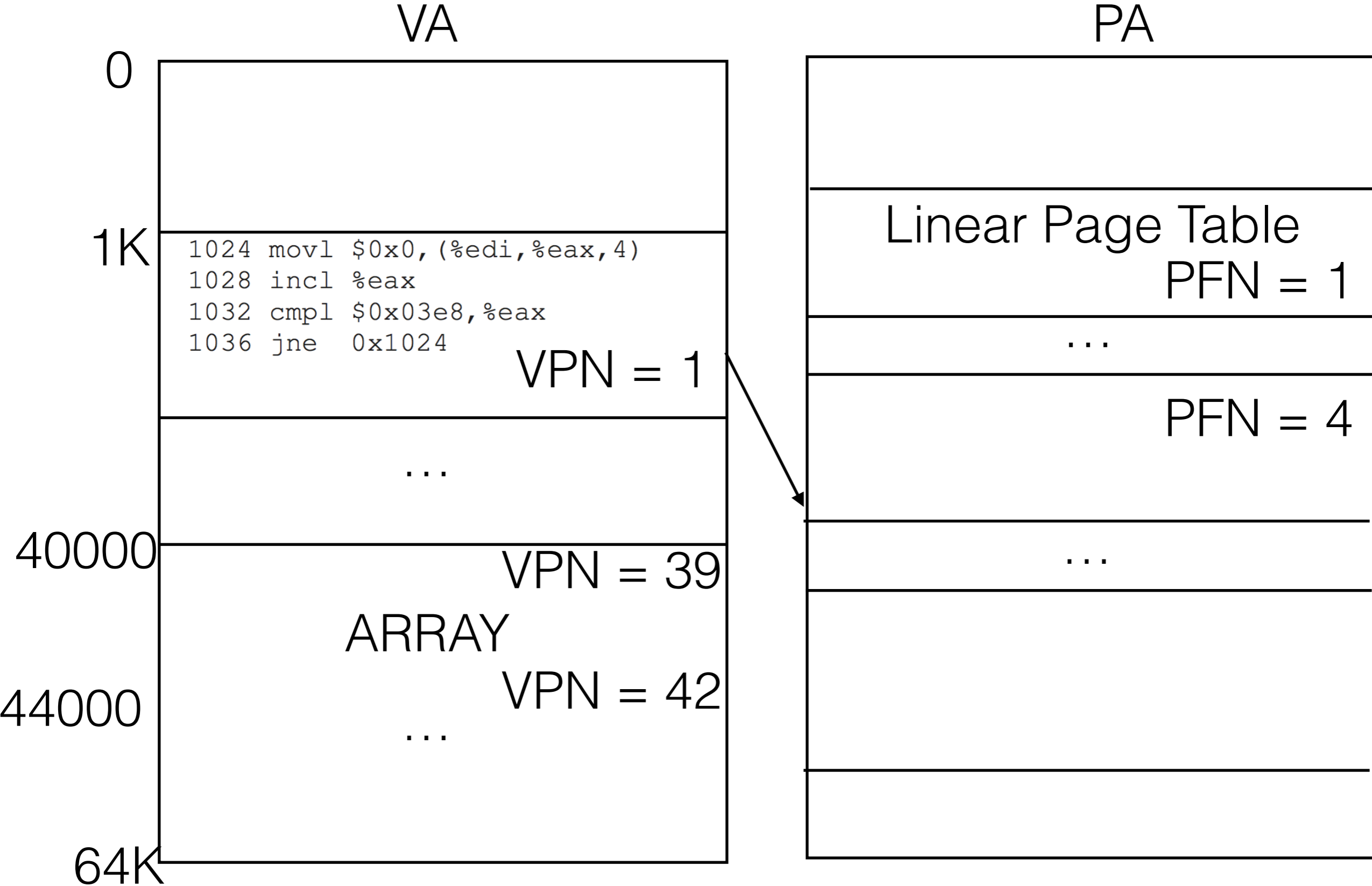
# Revision



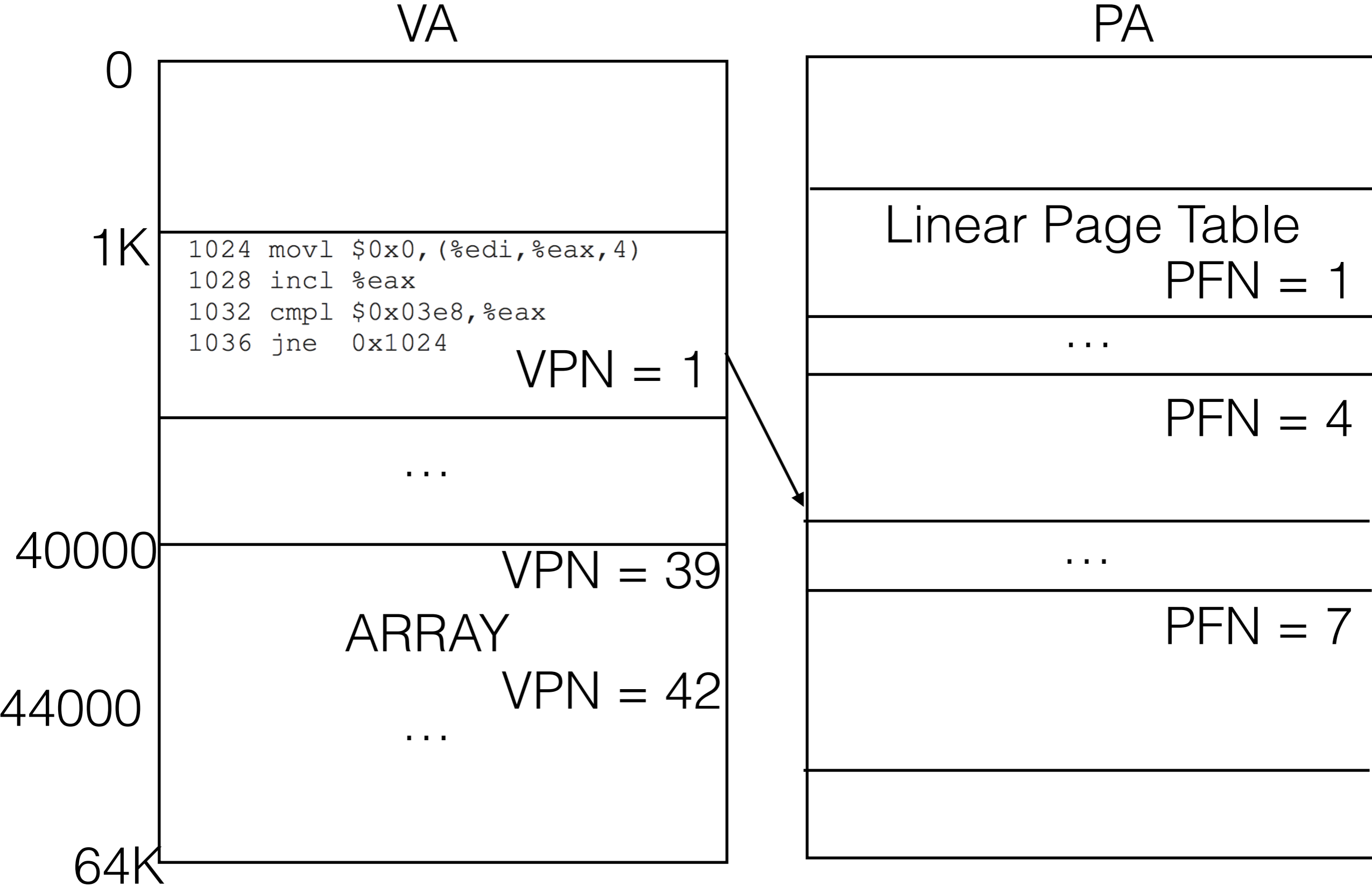
# Revision



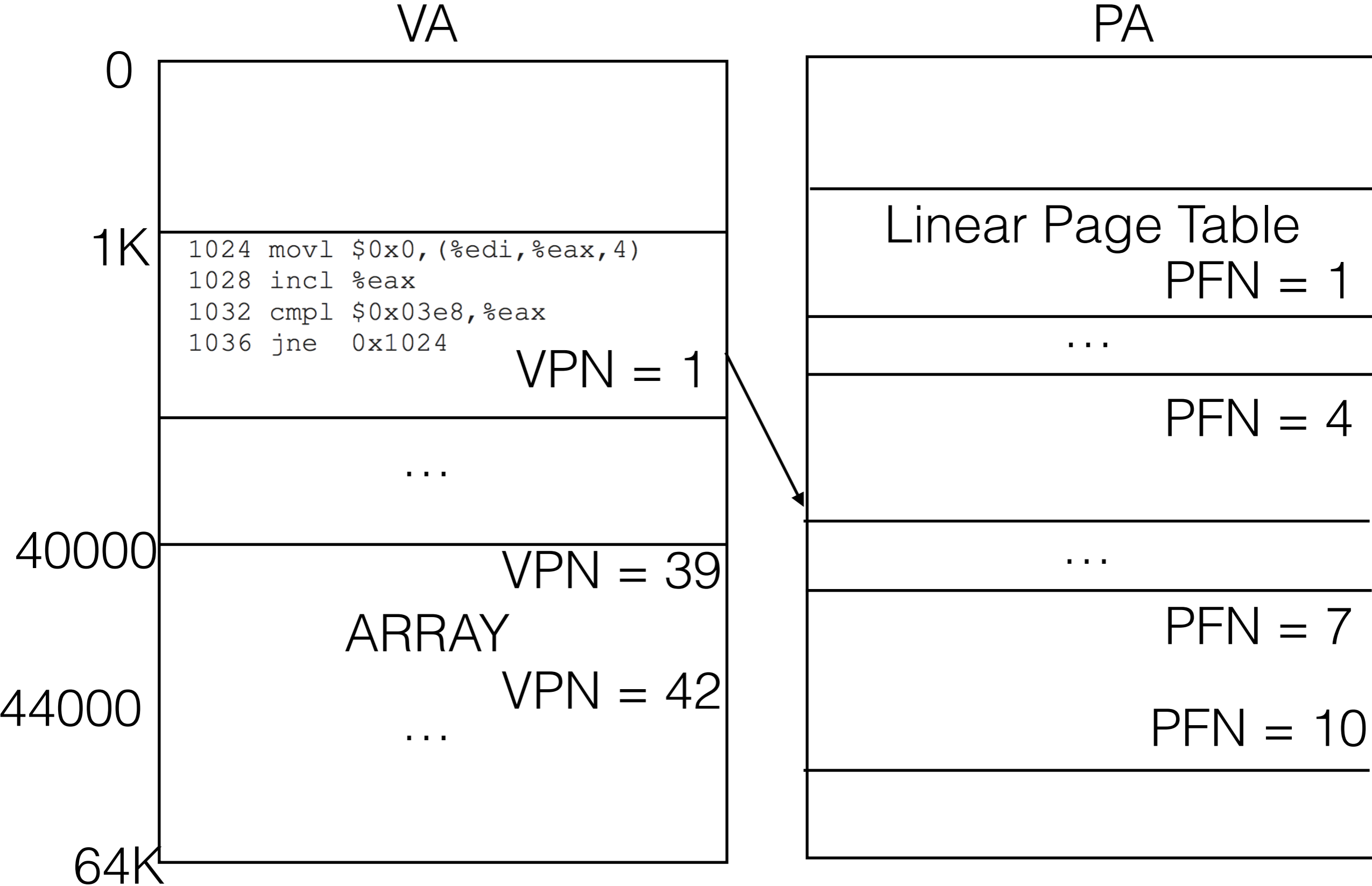
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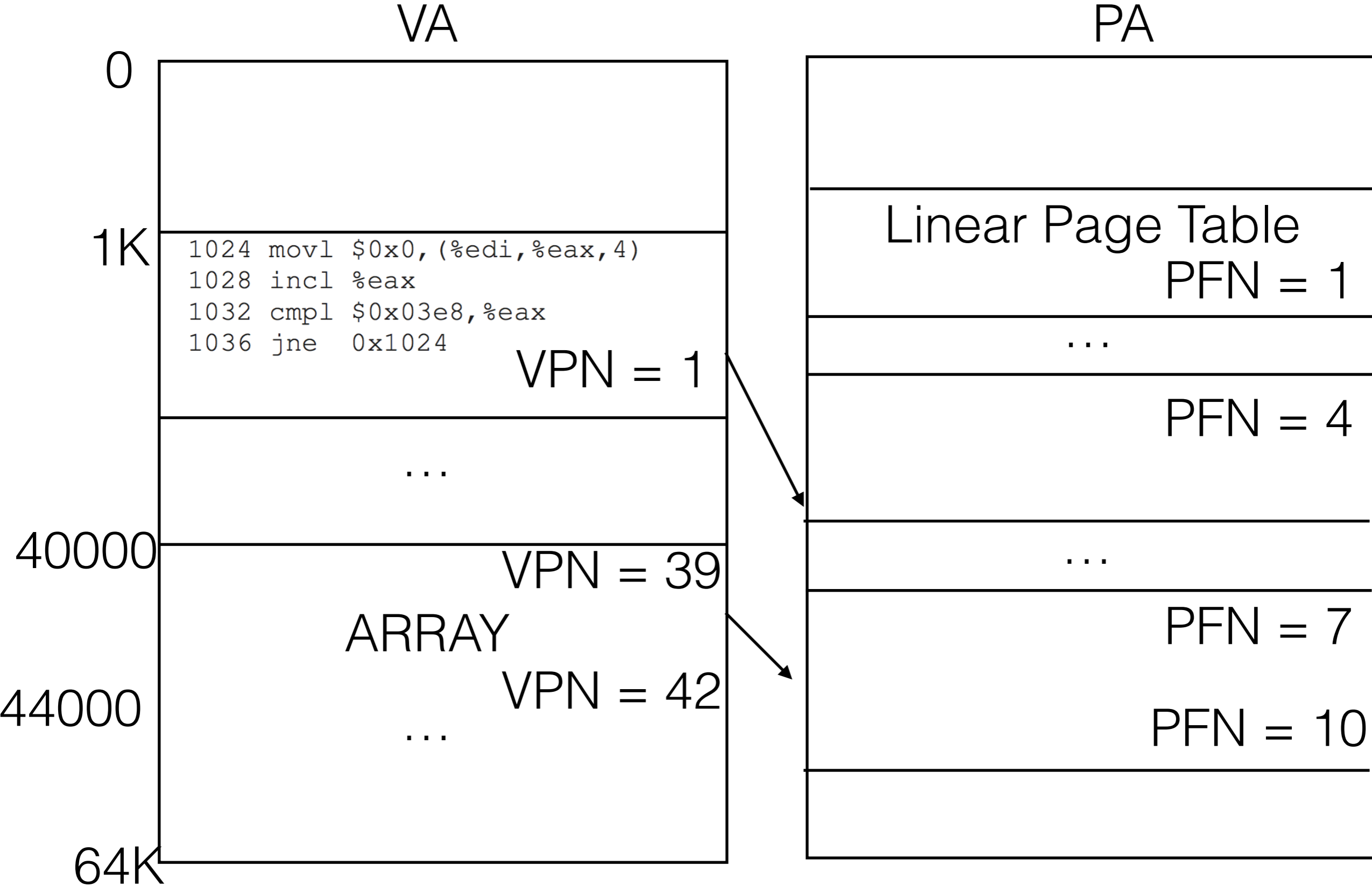


# Revision



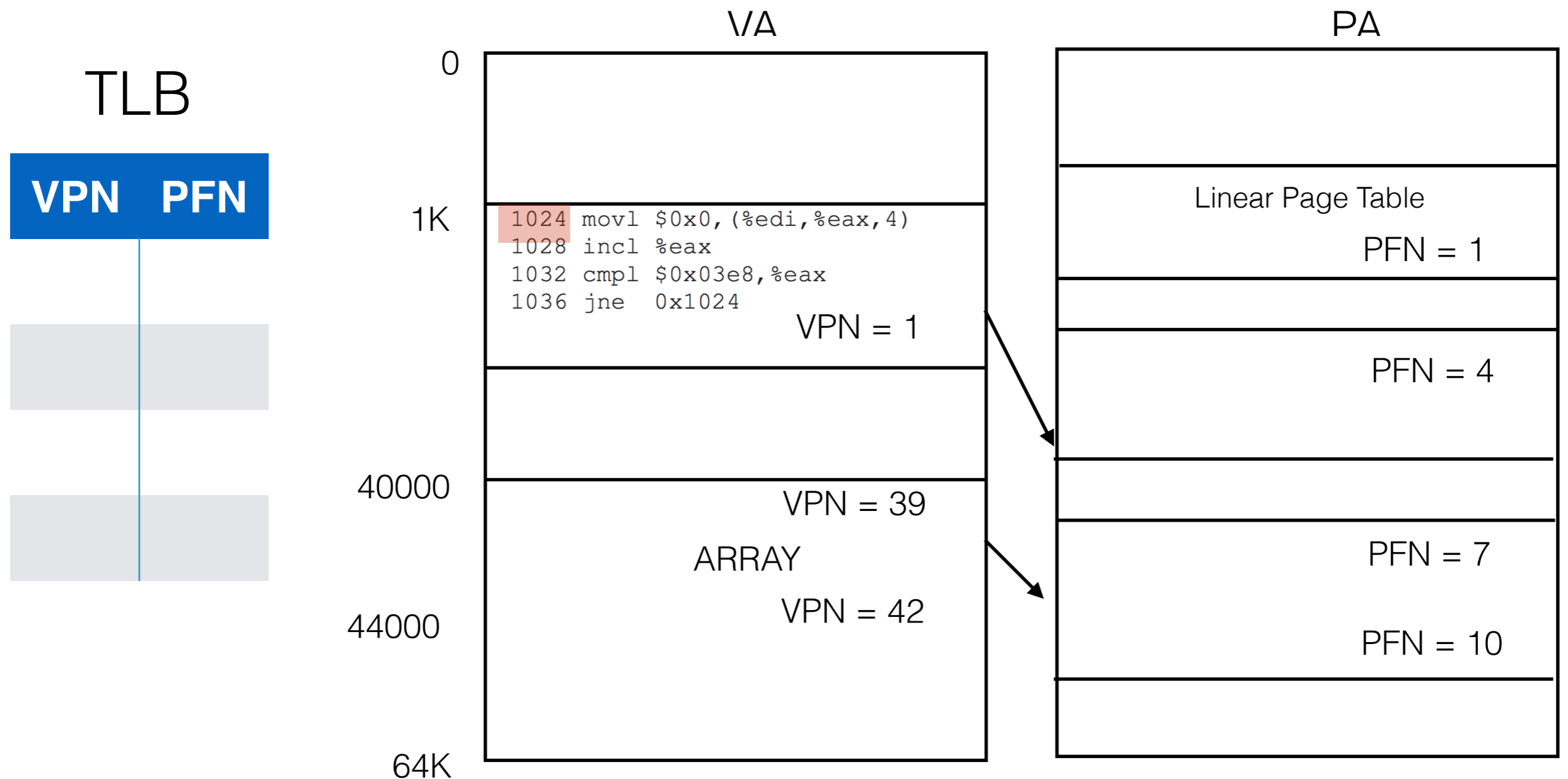


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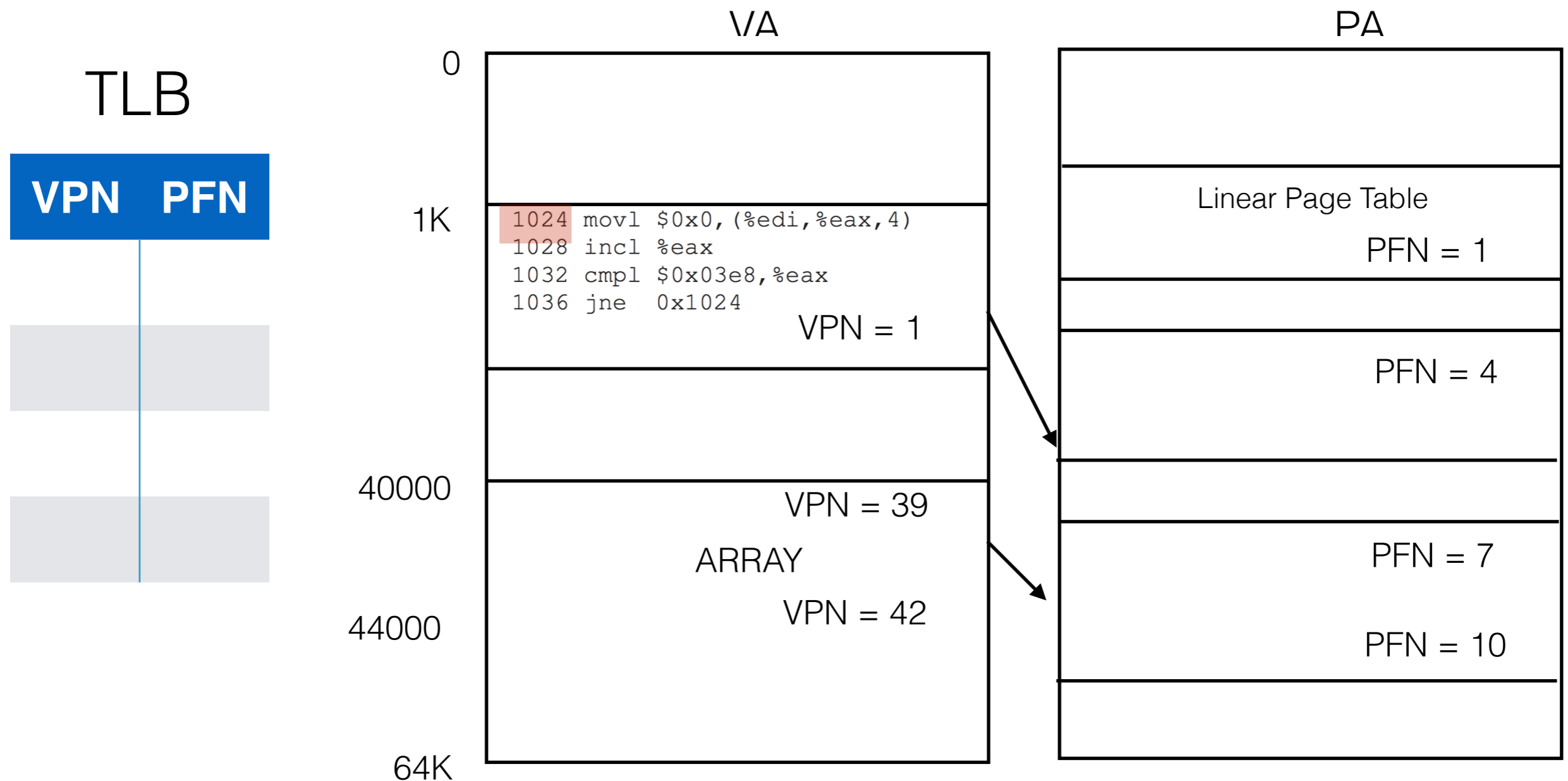
# Worked Out Example

## FETCH VA 1024



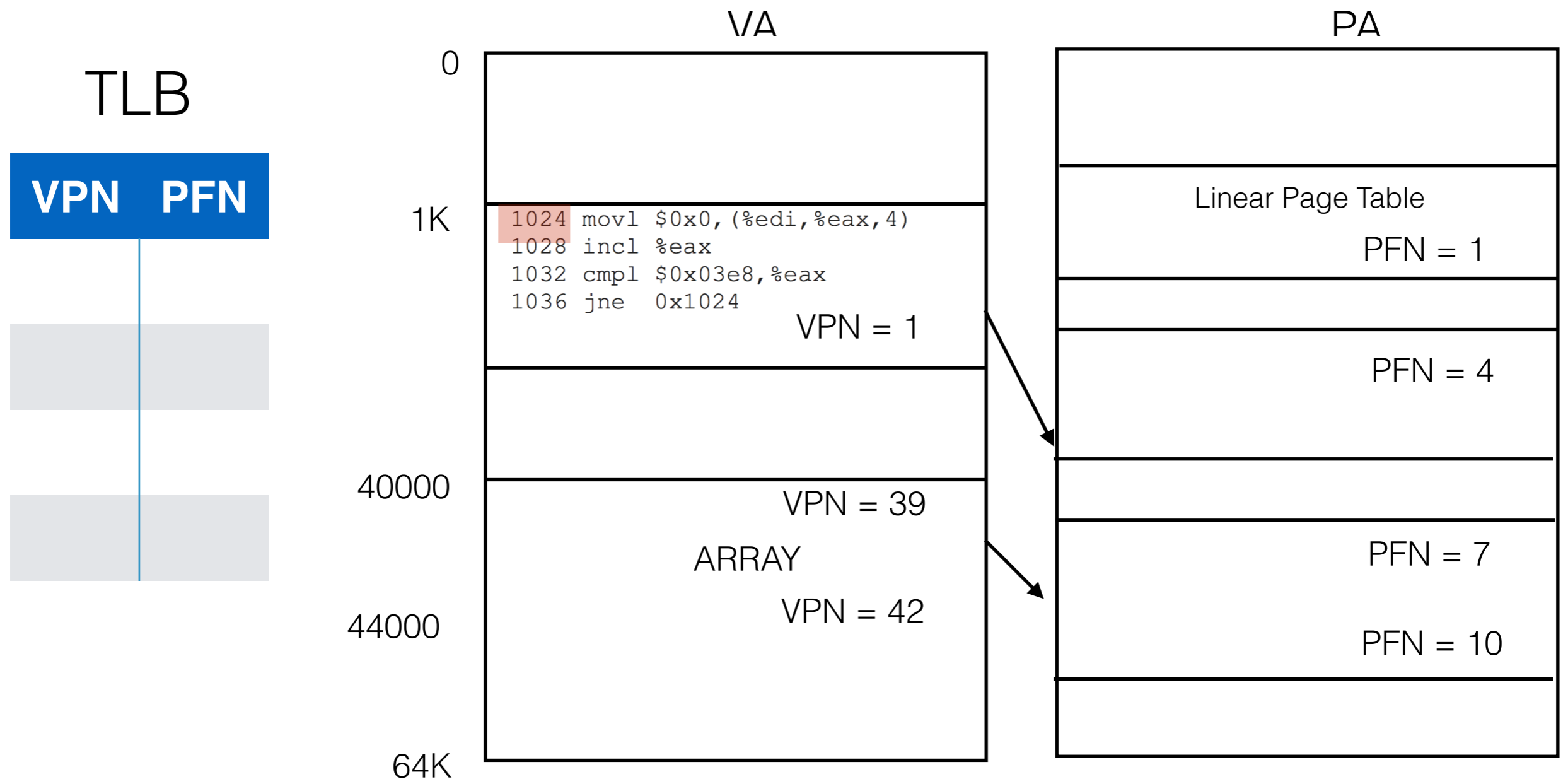
# Worked Out Example

Get VPN for VA 1024. VPN = 1



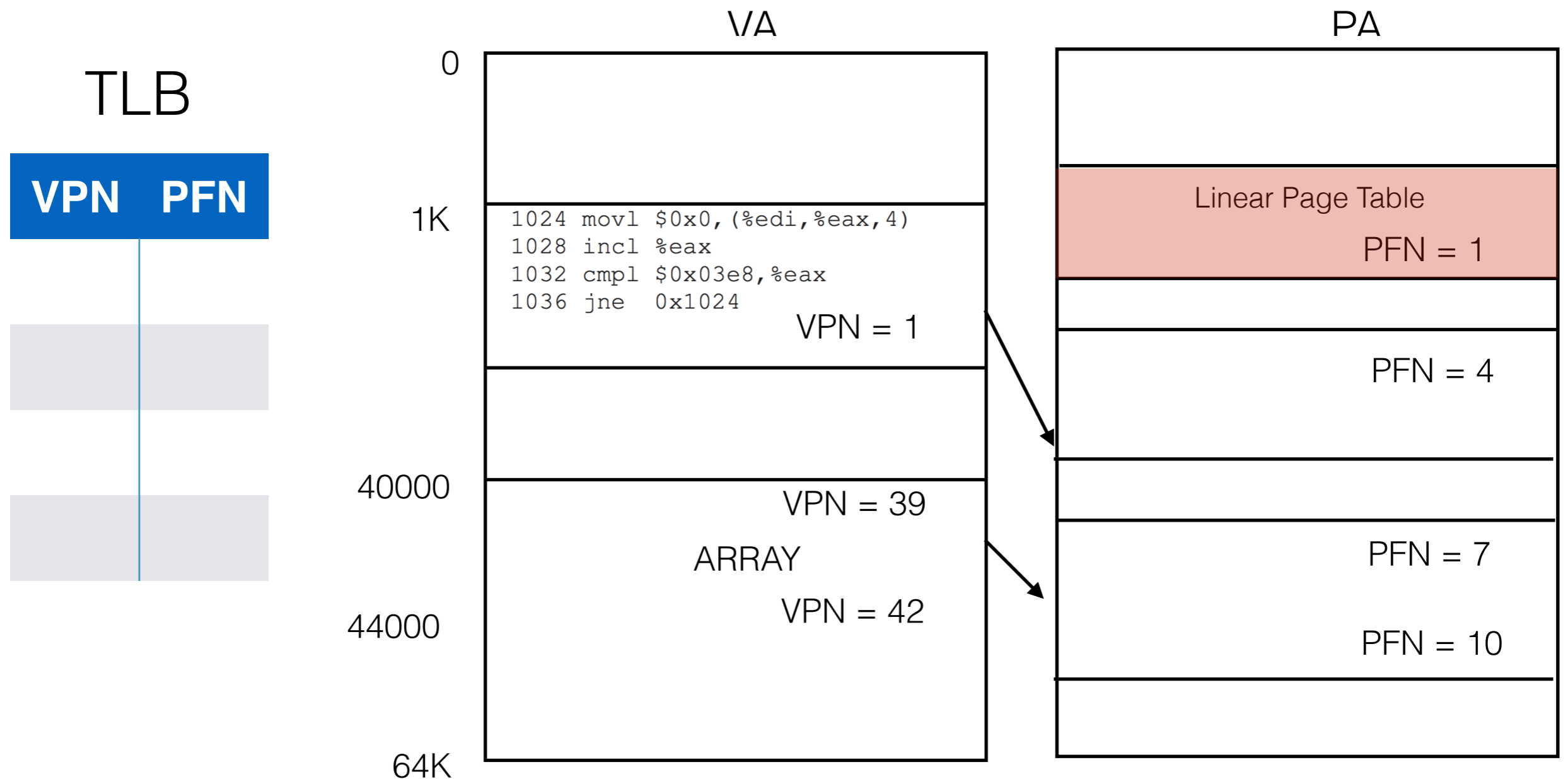
# Worked Out Example

**LOOK IN TLB for VPN = 1. Not found. TLB Miss!**



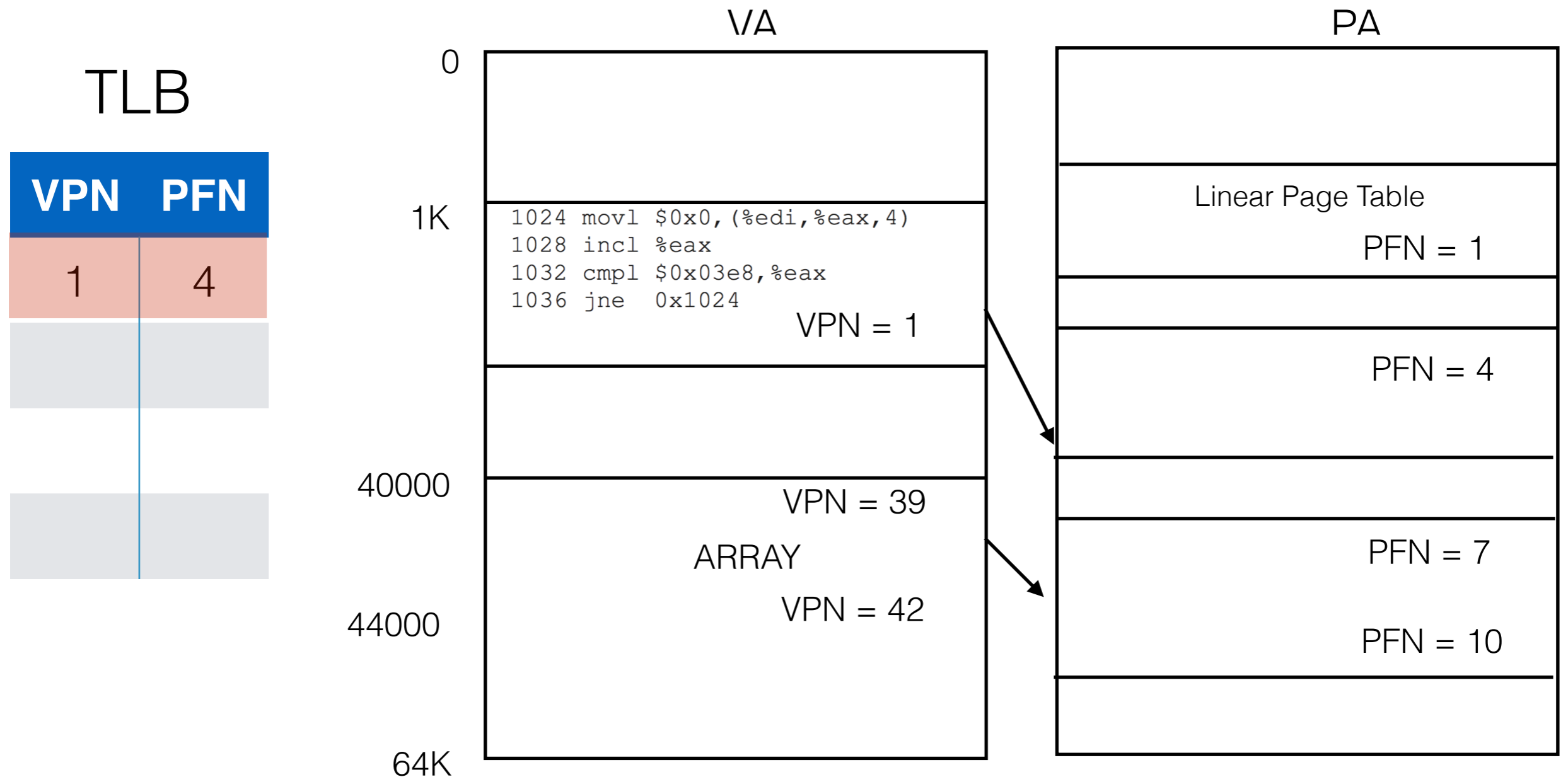
# Worked Out Example

Find PFN for VPN = 1 by accessing Page Table



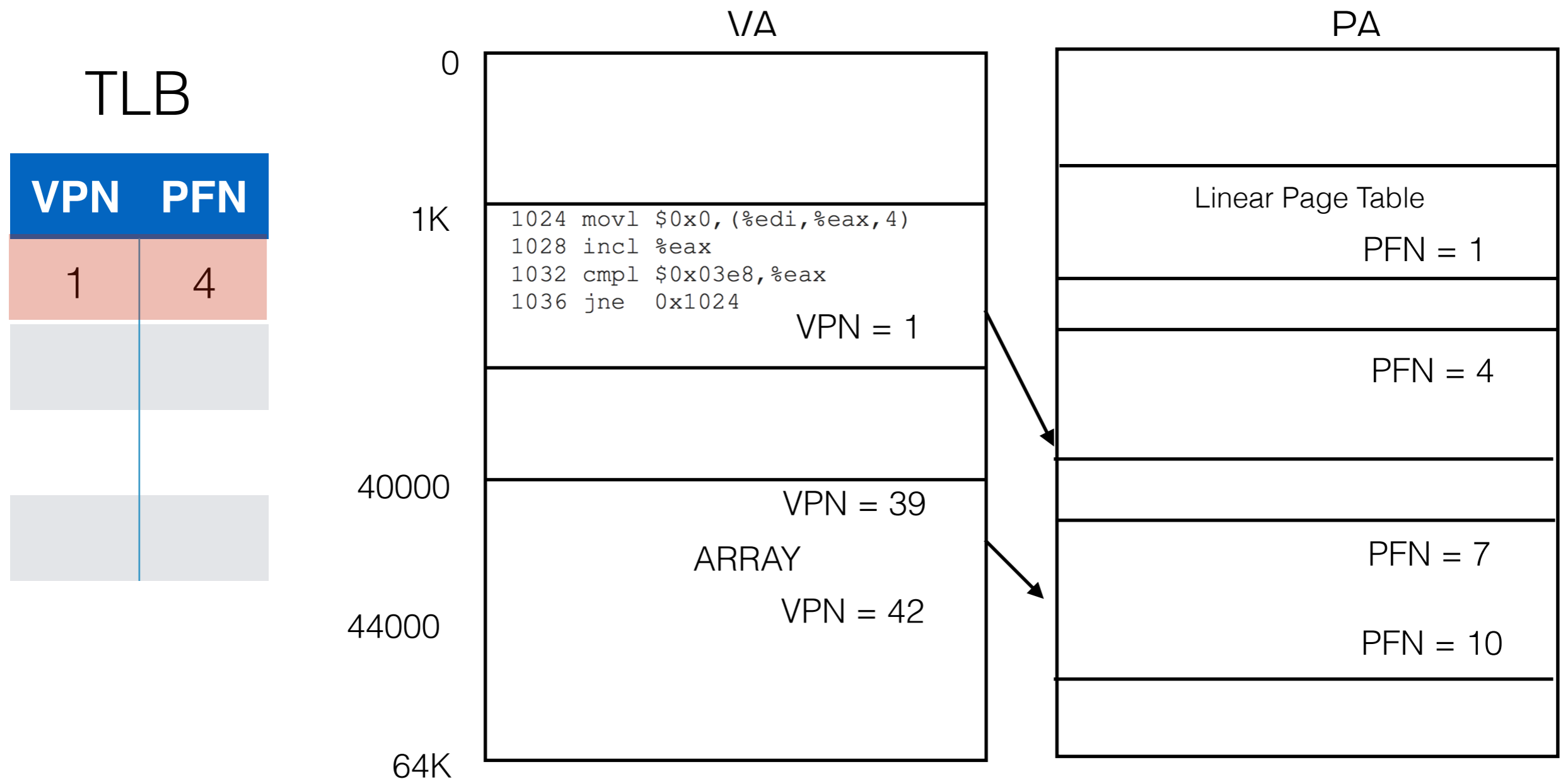
# Worked Out Example

## Add entry to TLB



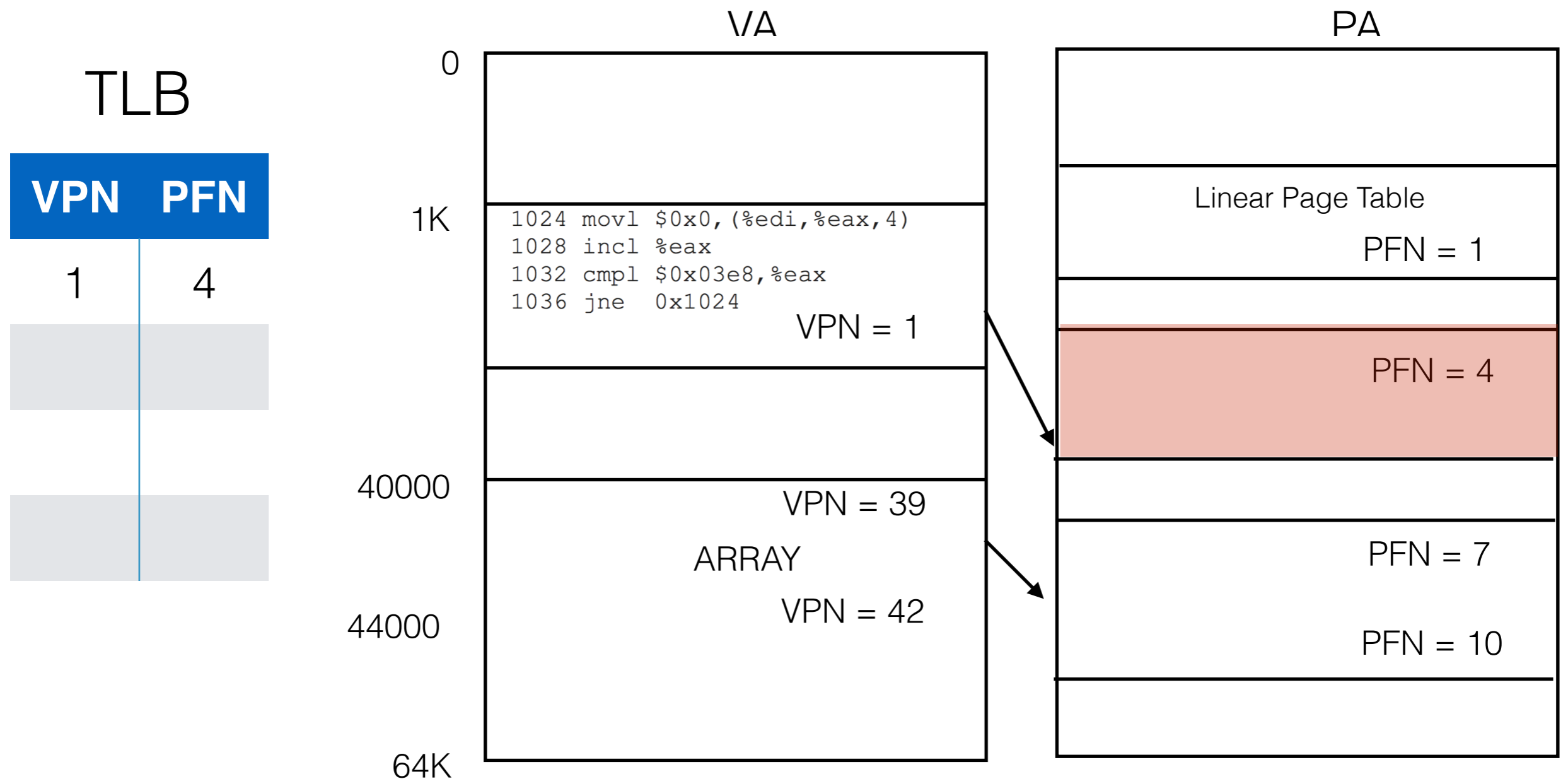
# Worked Out Example

## Search for translation of VPN = 1 on TLB



# Worked Out Example

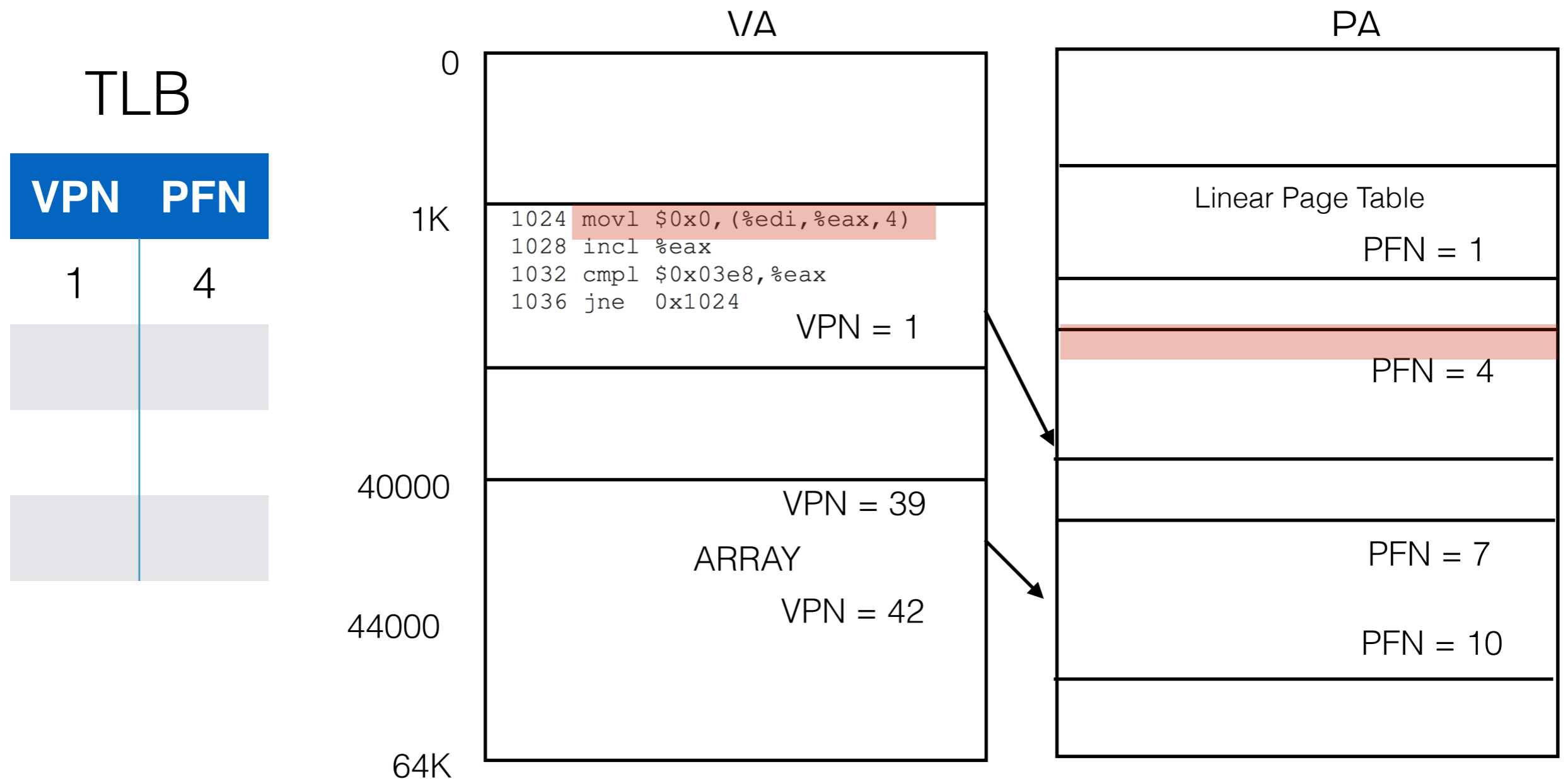
Goto PFN 4 and create PA by adding offset





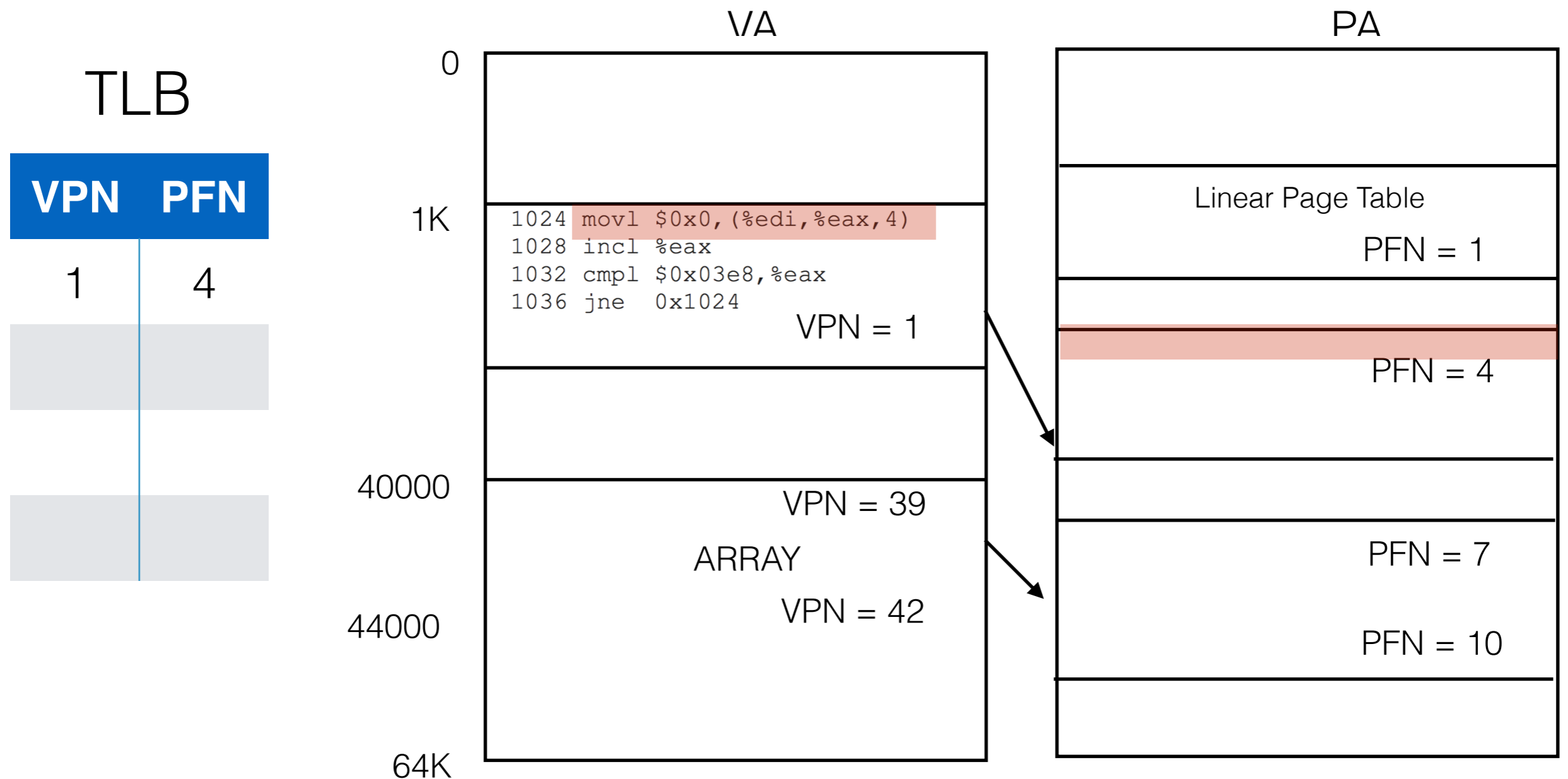
# Worked Out Example

## READ INSTRUCTION at PA(1024)



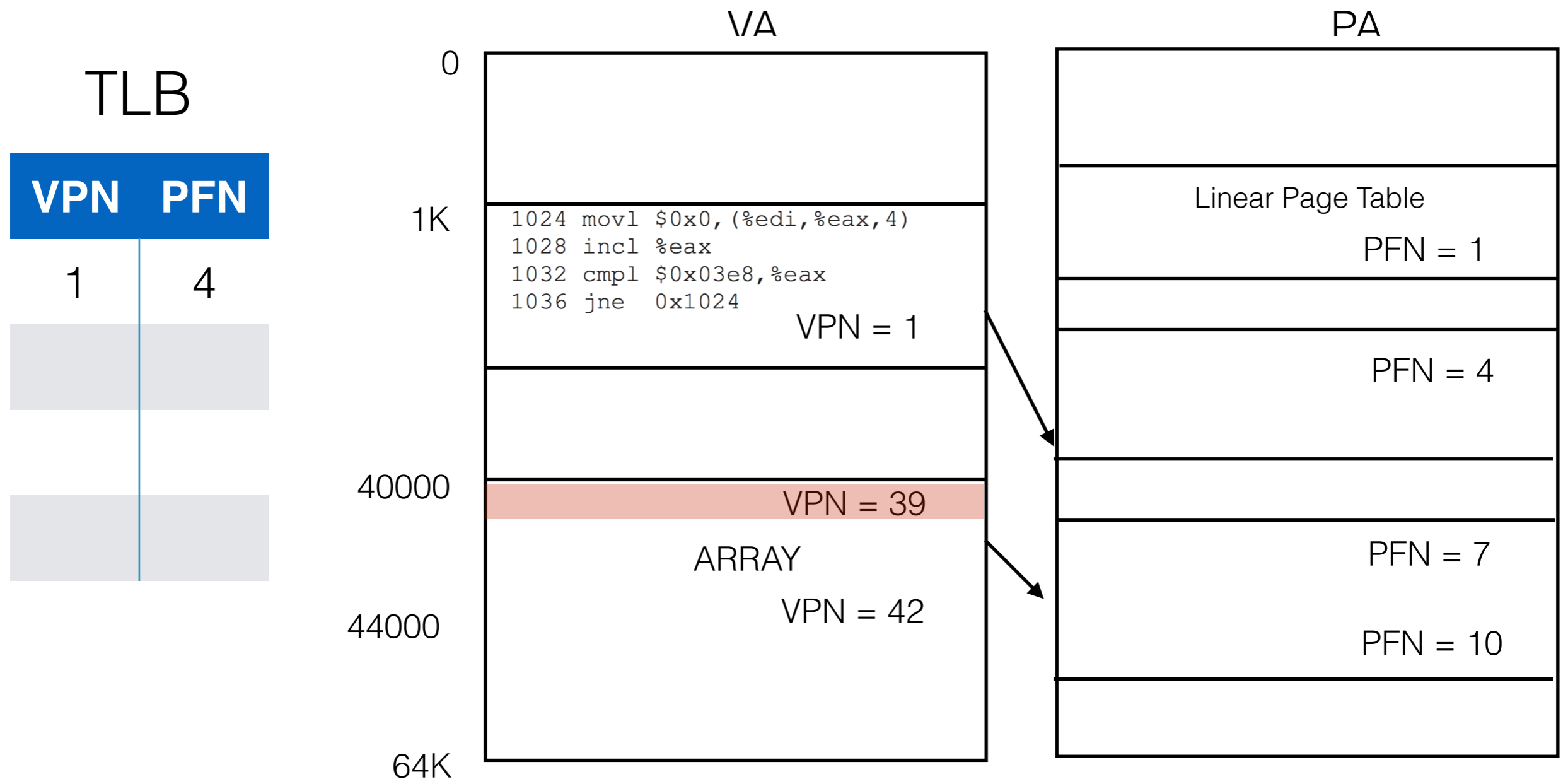
# Worked Out Example

## READ INSTRUCTION at PA(1024)



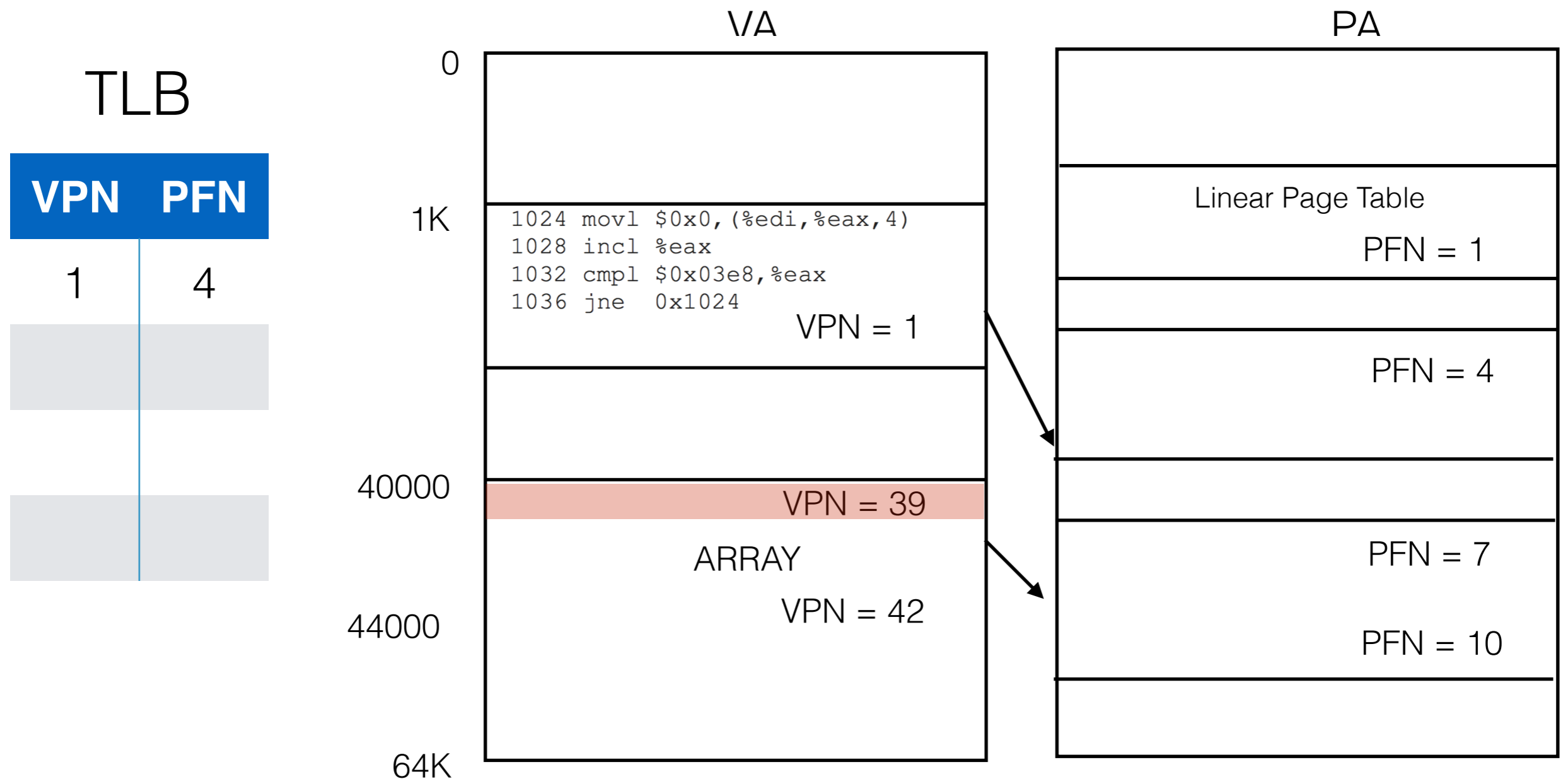
# Worked Out Example

Find  $EDI + 4 * EAX \rightarrow VA = 40000$



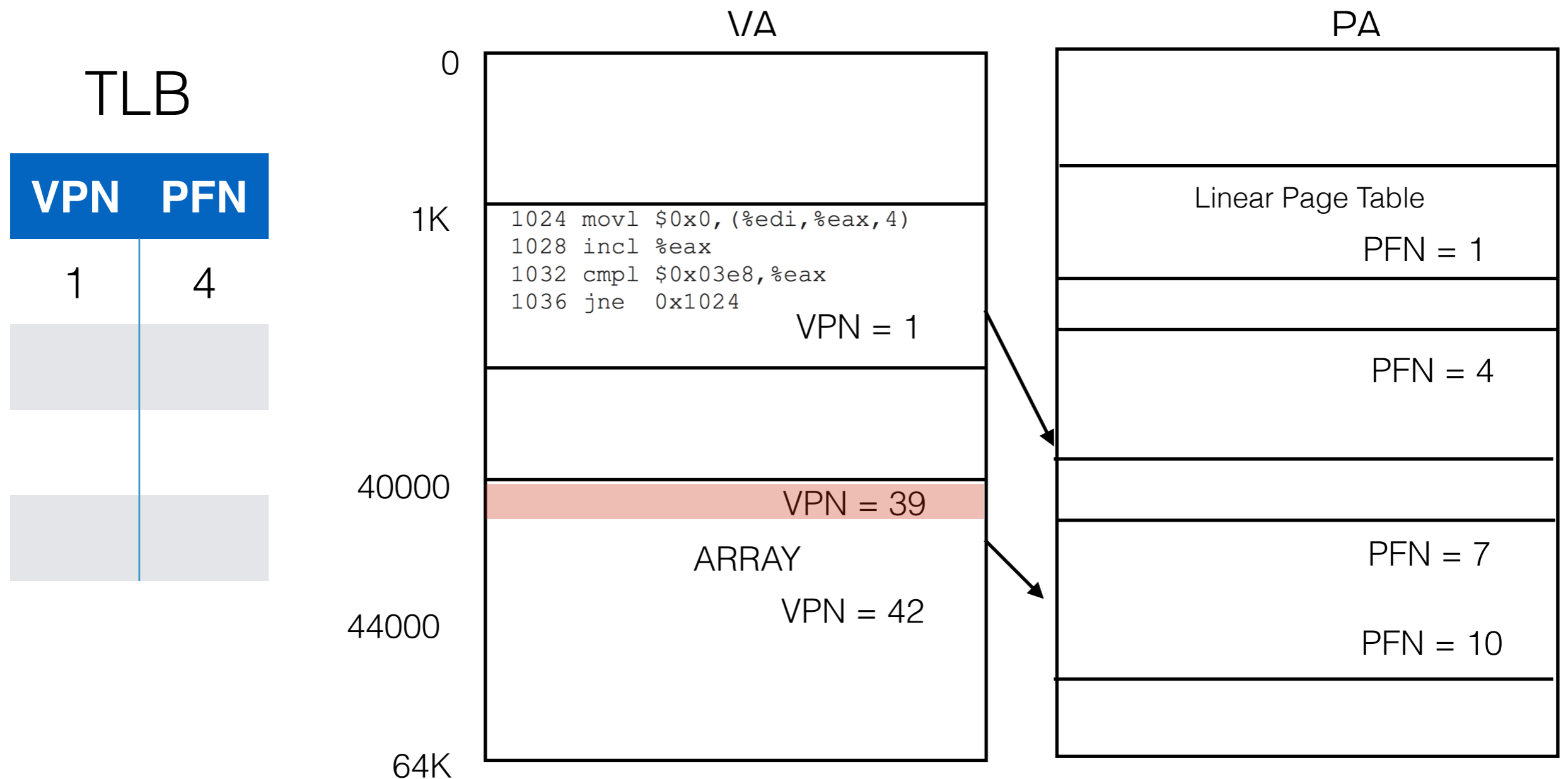
# Worked Out Example

Find VPN for VA 40000. VPN = 39



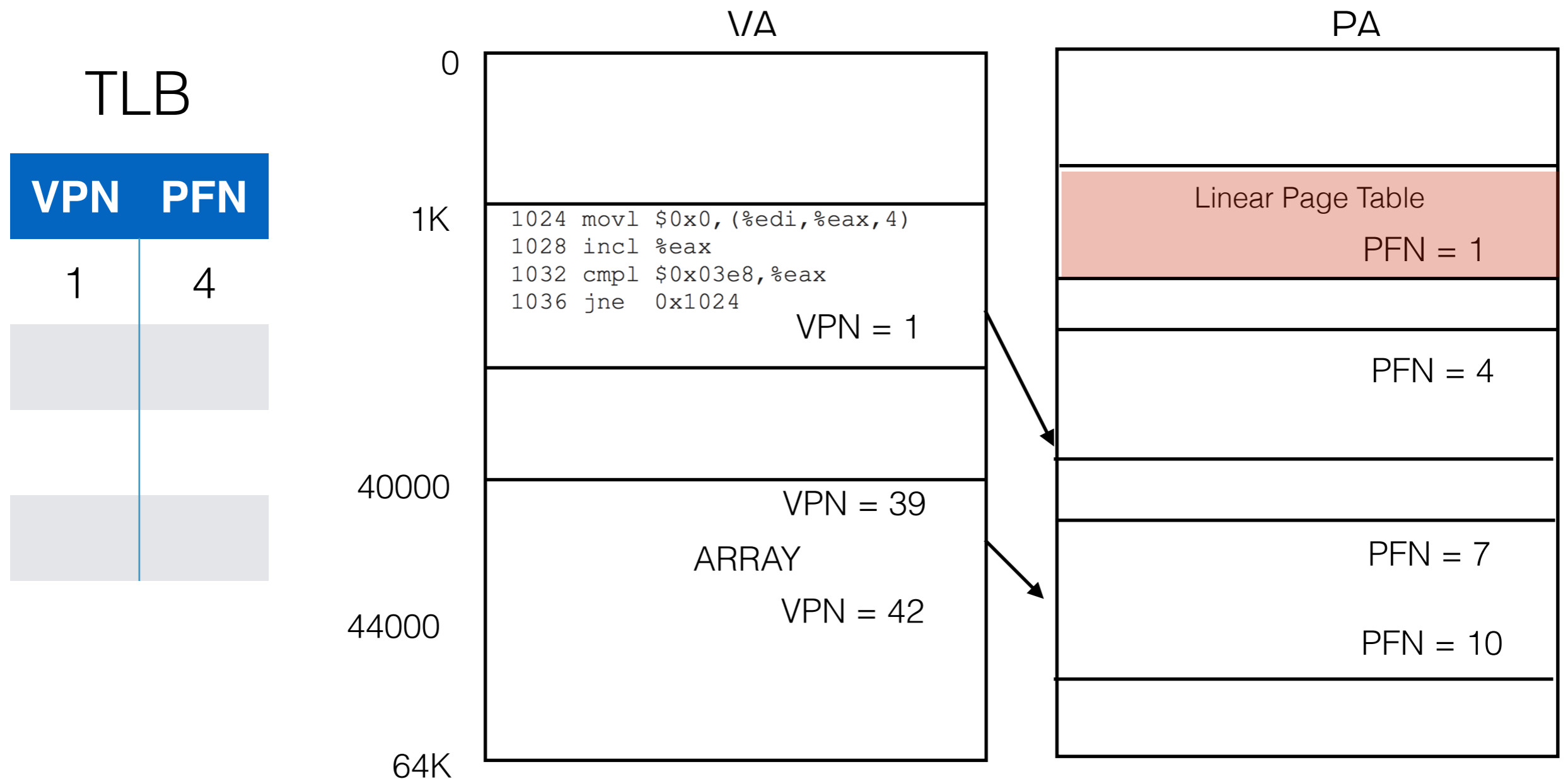
# Worked Out Example

Check TLB for VPN = 39. Miss!



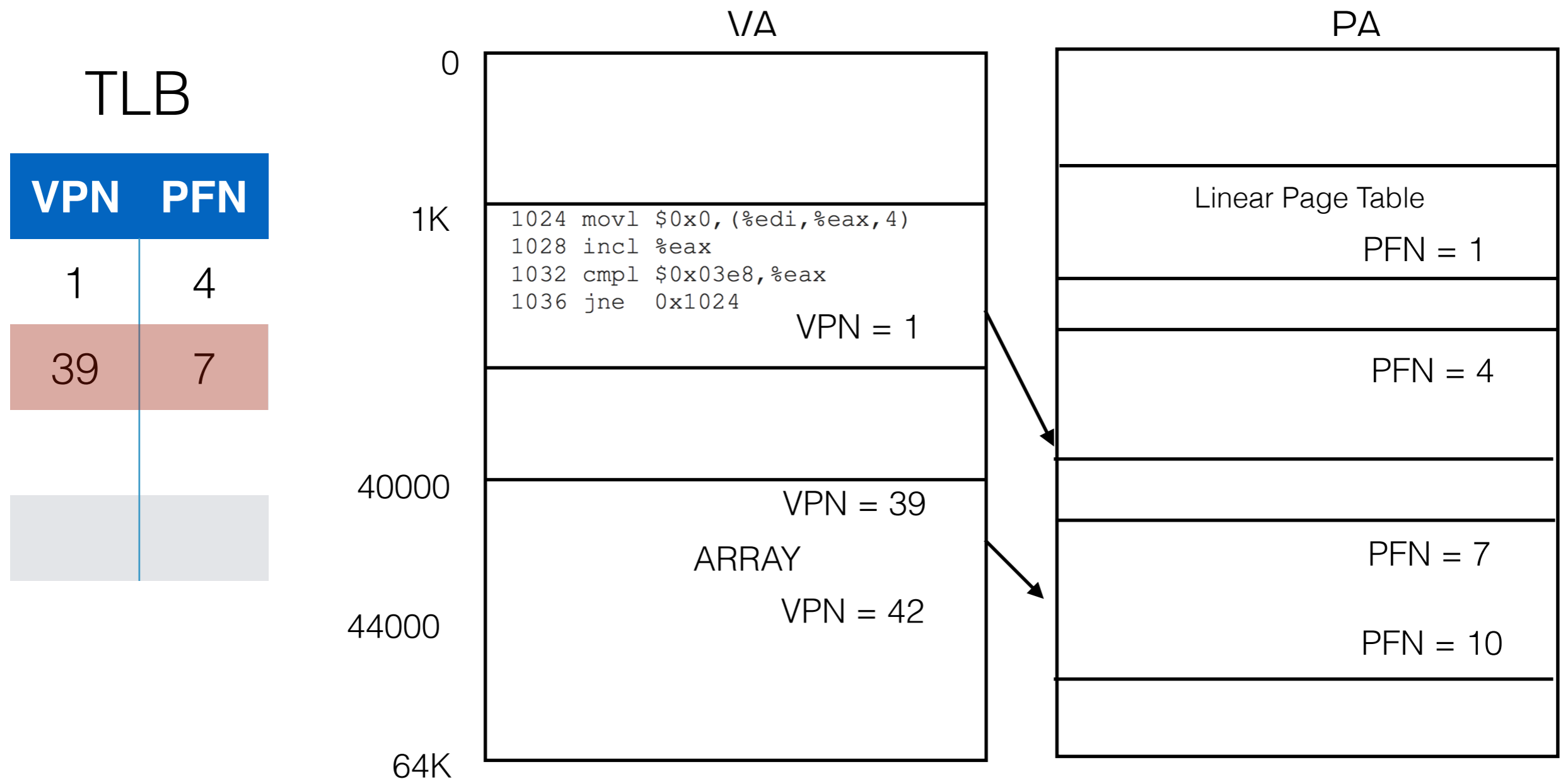
# Worked Out Example

## Get PFN for VPN = 39 from Page Table



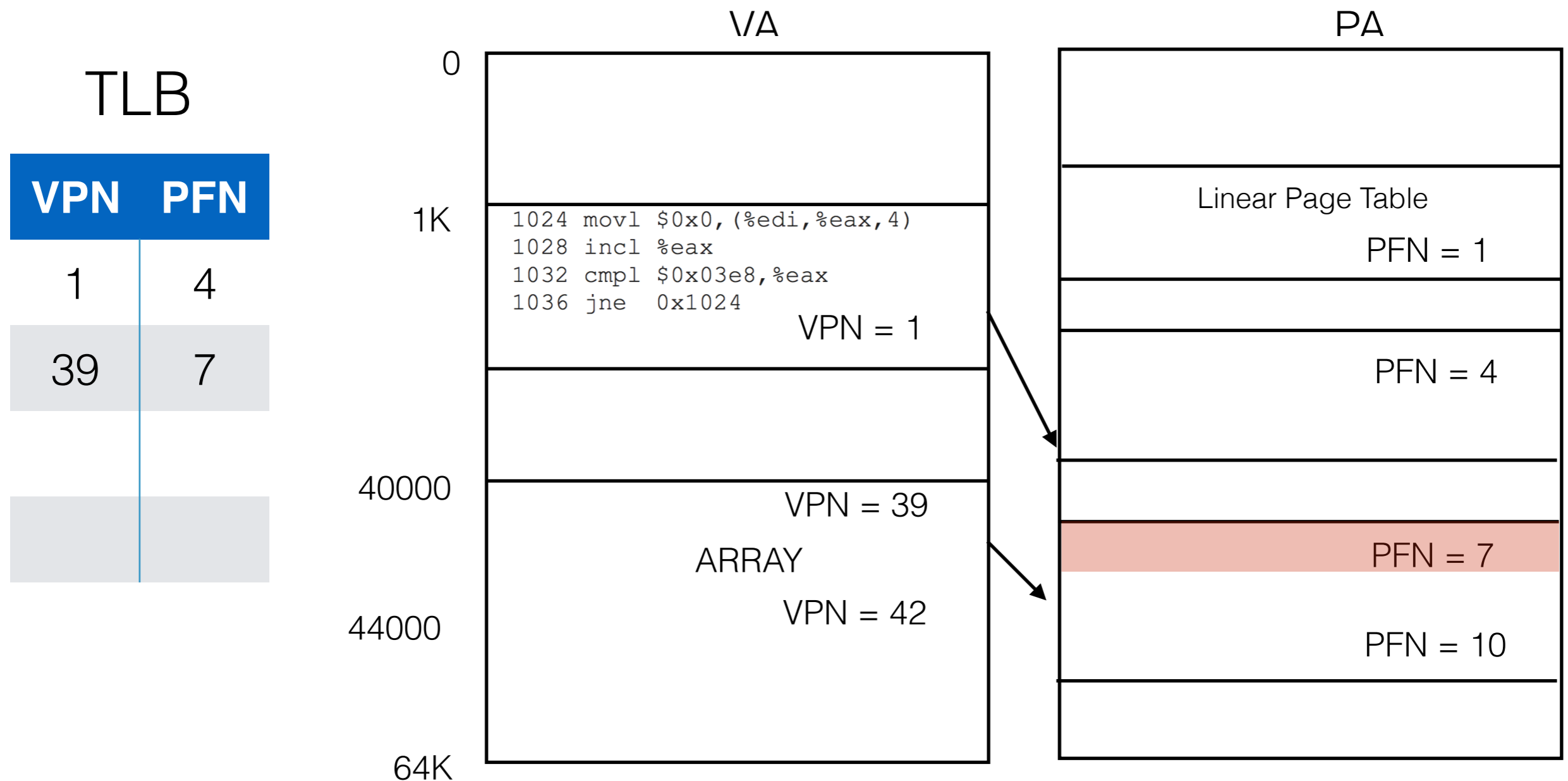
# Worked Out Example

## Store translation in TLB



# Worked Out Example

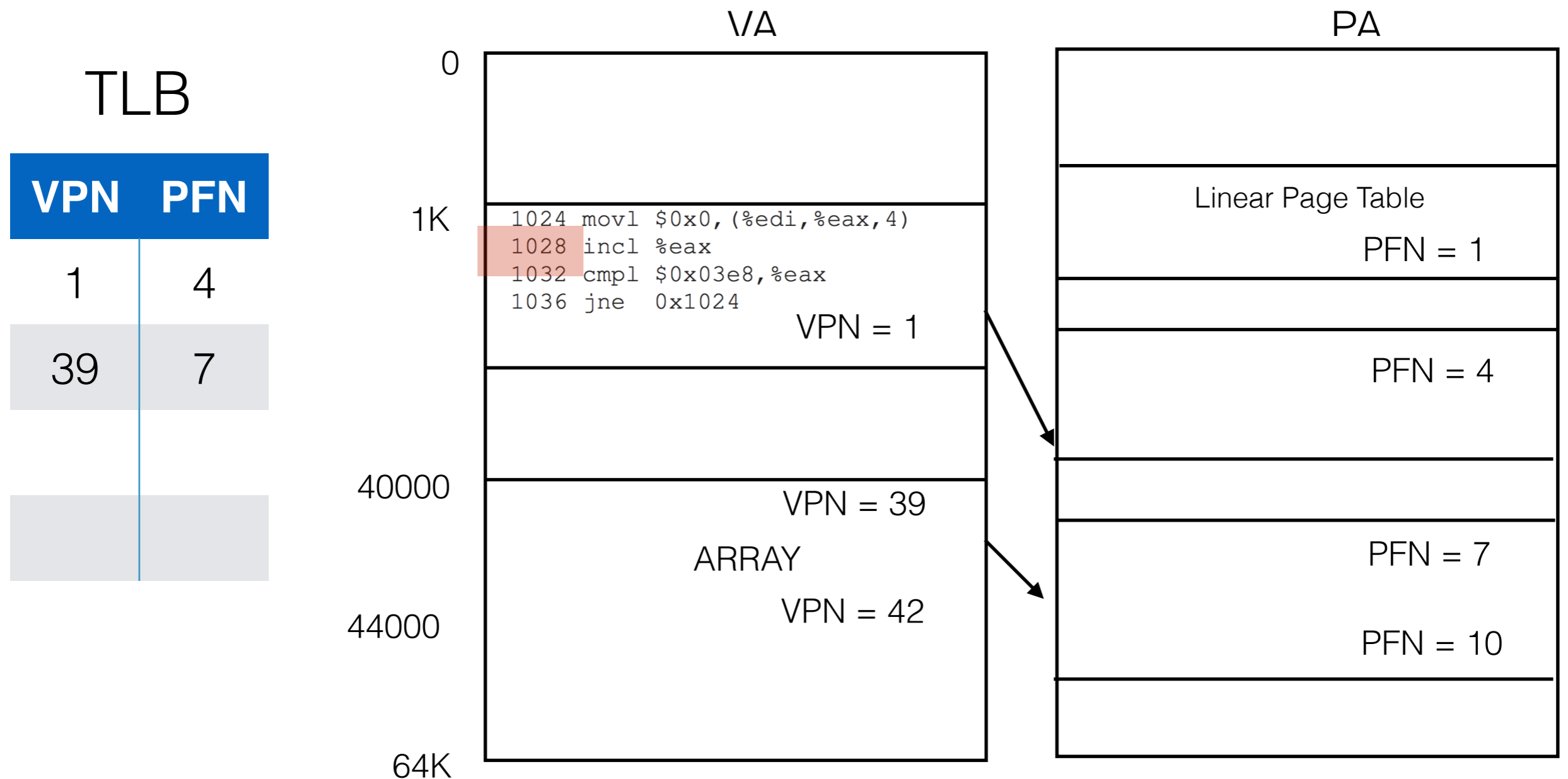
Find PFN of VPN = 39 from TLB. Add offset to get PA.





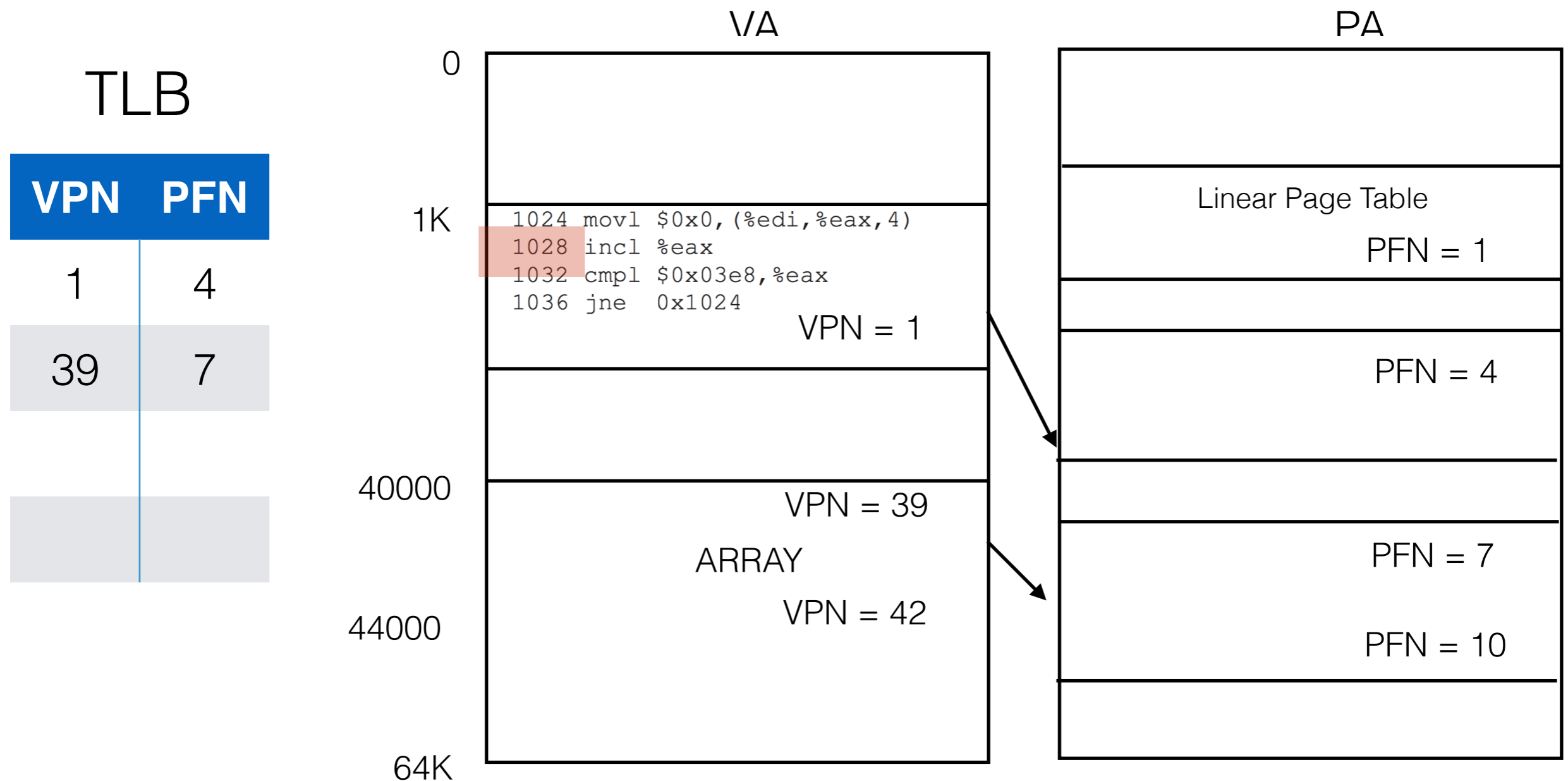
# Worked Out Example

## FIND PA FOR VA = 1028



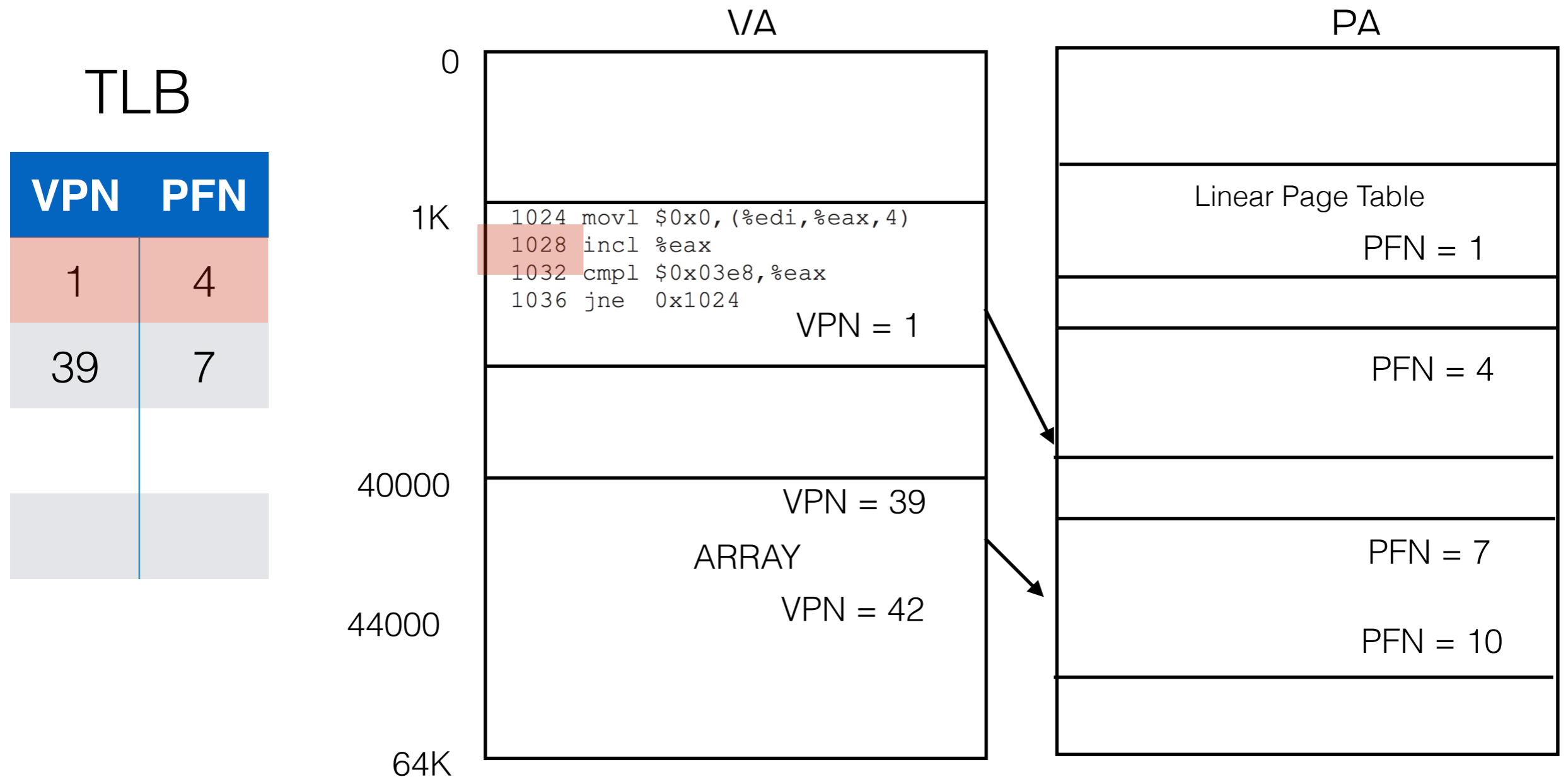
# Worked Out Example

VPN = 1. Find Translation in TLB for VPN = 1. Found!



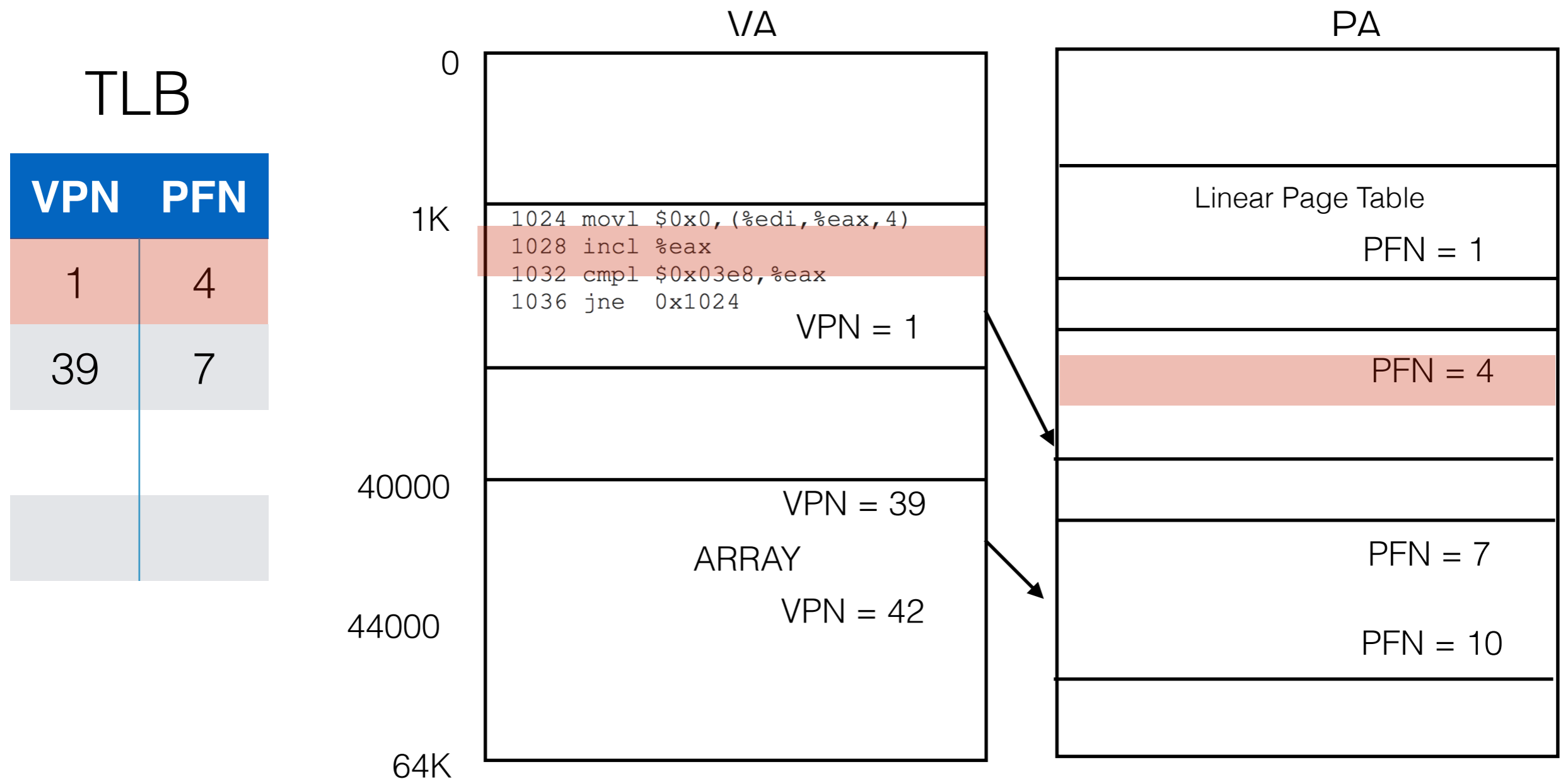
# Worked Out Example

$$\text{PFN} = \text{TLB}[1] = 4$$



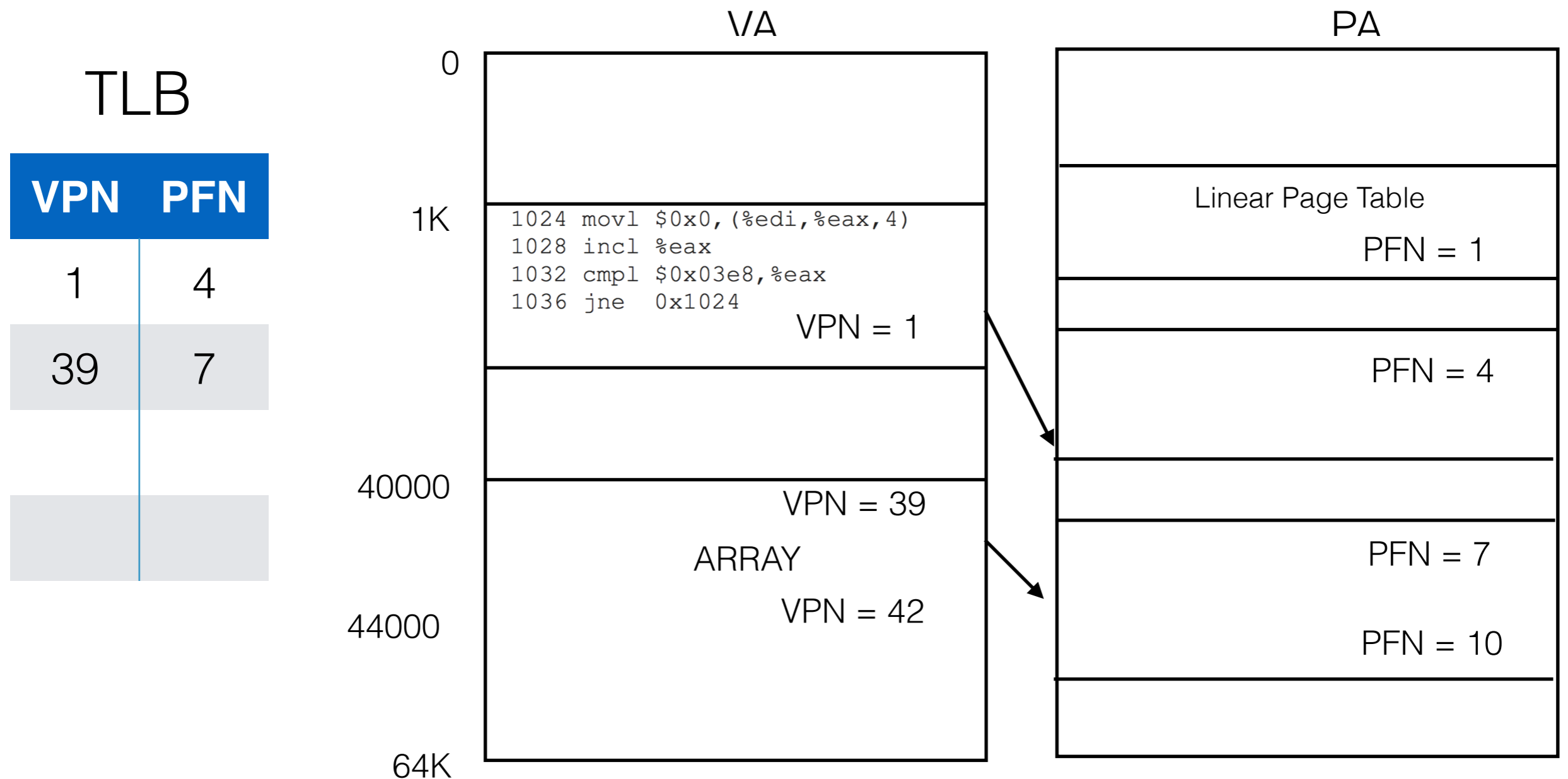
# Worked Out Example

Get PA by adding offset to PFN = 4 and execute



# Worked Out Example

## TLB miss for VPN = 40...



# Spatial and Temporal Locality

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  2. Instructions are spatially close (1024, ...)
3. Temporal locality -> TLB has a good hit rate
  1. Loop. Re-using same instructions which exist in TLB

# Context Switch

---

TLB

VPN	PFN
1	4
39	7

# Context Switch

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TLB

P1 running

VPN	PFN
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TLB

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VPN	PFN
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P2 running



# Context Switch

---

## TLB

P1 running

VPN	PFN
1	4
39	7
...	...
1	30

---

P2 running

# Context Switch

---

## TLB

P1 running

VPN	PFN
1	4
39	7
...	...
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P2 running

What will VPN 1 be mapped to?

# Context Switch

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## TLB

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39	7
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P2 running

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## TLB

P1 running

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P2 running

What will VPN 1 be mapped to?

# Context Switch

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## TLB

P1 running

---

VP N	PFN	VALID	PERMISSION	ASID
1	4	1	R	1
39	7	1	R	1
...	...	0	RW	
1	30	1	RWX	2

P2 running

# TLB Entry Replacement

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      1. TLB size = N

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2. When to replace?
  1. Newer translation found
  2. Context switch
3. How to replace?
  1. Remove at random
  2. Remove least recently used (LRU)
    1. Corner case:
      1. TLB size =  $N$
      2.  $N+1$  page accesses in loop

# Memory Virtualisation Thus Far

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  - Cons: Slow, lots of memory accesses; memory overhead/  
process is huge!

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- Paging + TLB

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  - Pros: Very low chances of segmentation
  - Cons: Slow, lots of memory accesses; memory overhead/process is huge!
- Paging + TLB
  - Pros: Improves the address translation speed (spatial & temporal locality)
  - Cons: Limited in size, memory overhead/process still huge



# Reducing Memory Overheads of Paging

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- 32 bit address space with 4 KB pages

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- Remaining bits =  $32 - 12 = 20$

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  - # pages =  $2^{20}$

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- 32 bit address space with 4 KB pages
- 4 KB pages  $\rightarrow$  12 bits?
- Remaining bits =  $32 - 12 = 20$ 
  - 20 bit VPN
  - # pages =  $2^{20}$
- 4 bytes per translation  $\rightarrow 4 * 2^{20}$  MB = **4 MB/process**

# Reducing Memory Overheads of Paging

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Solution 0: Decrease the size of VA space

# Reducing Memory Overheads of Paging

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- 12 bit offset for 4 K pages
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- 12 bit offset for 4 K pages
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- 4 bytes per translation  $\rightarrow 4 * 2^{18} \text{ MB} = \mathbf{1 \text{ MB/process}}$

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## Solution 0: Decrease the size of VA space

- 12 bit offset for 4 K pages
- 30 bit address space
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- 4 bytes per translation  $\rightarrow 4 * 2^{18} \text{ MB} = \mathbf{1 \text{ MB/process}}$
  
- 32 bit address space  $\rightarrow 4 \text{ GB}$

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- 12 bit offset for 4 K pages
- 30 bit address space
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- 4 bytes per translation  $\rightarrow 4 * 2^{18} \text{ MB} = \mathbf{1 \text{ MB/process}}$
  
- 32 bit address space  $\rightarrow 4 \text{ GB}$
- 30 bit address space  $\rightarrow 1 \text{ GB}$

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Solution 1: Increase the page size

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- 32 bit address space with 16 KB pages

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- 16 KB pages -> 14 bits?

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- 32 bit address space with 16 KB pages
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- 32 bit address space with 16 KB pages
- 16 KB pages  $\rightarrow$  14 bits?
- Remaining bits =  $32 - 14 = 18$ 
  - 18 bit VPN

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- 32 bit address space with 16 KB pages
- 16 KB pages  $\rightarrow$  14 bits?
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  - 18 bit VPN
  - # pages =  $2^{18}$

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## Solution 1: Increase the page size

- 32 bit address space with 16 KB pages
- 16 KB pages  $\rightarrow$  14 bits?
- Remaining bits =  $32 - 14 = 18$ 
  - 18 bit VPN
  - # pages =  $2^{18}$
- 4 bytes per translation  $\rightarrow 4 * 2^{18}$  MB = **1 MB/process**

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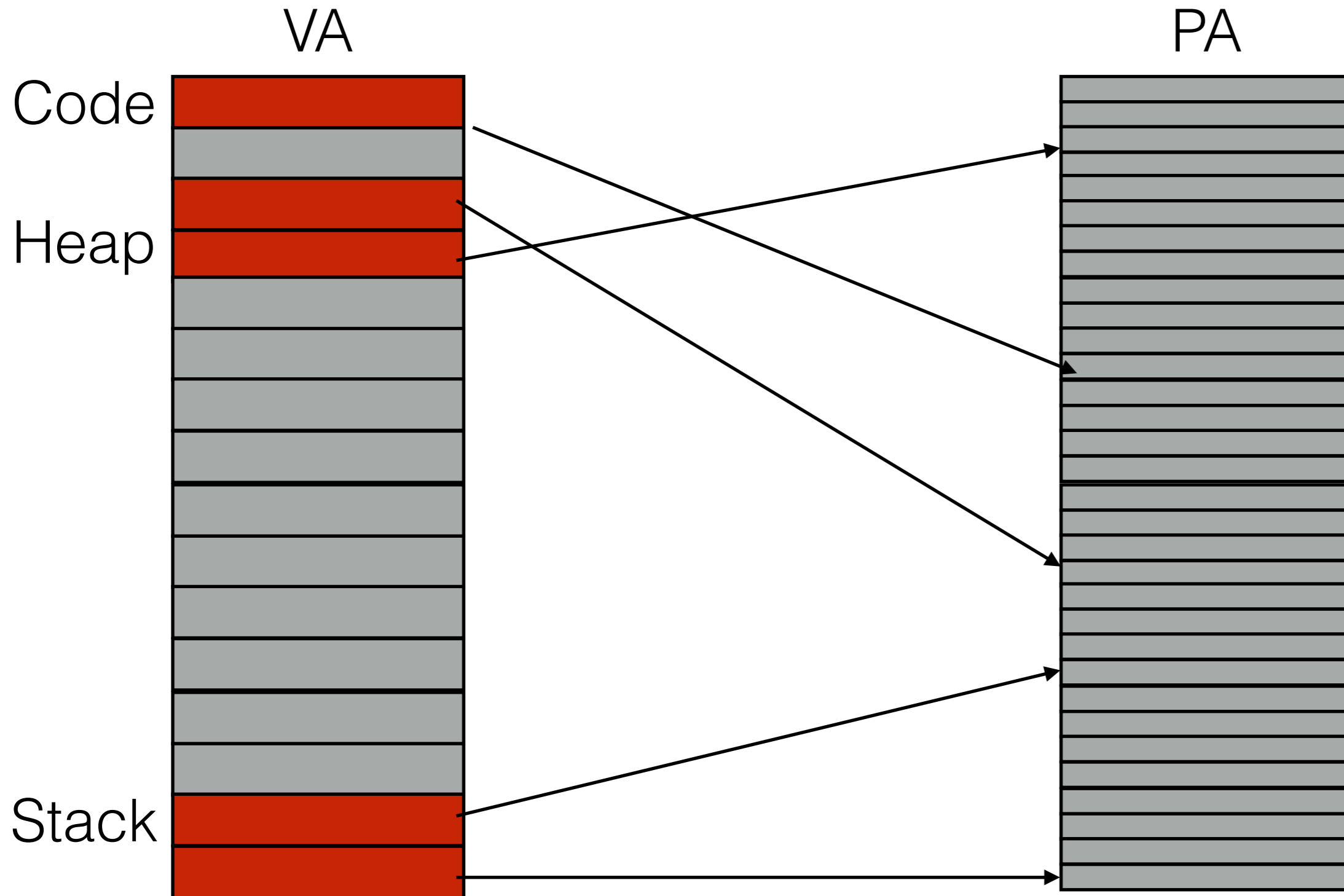
- 32 bit address space with 16 KB pages
- 16 KB pages  $\rightarrow$  14 bits?
- Remaining bits =  $32 - 14 = 18$ 
  - 18 bit VPN
  - # pages =  $2^{18}$
- 4 bytes per translation  $\rightarrow 4 * 2^{18}$  MB = **1 MB/process**

Larger page size  $\rightarrow$  Fragmentation



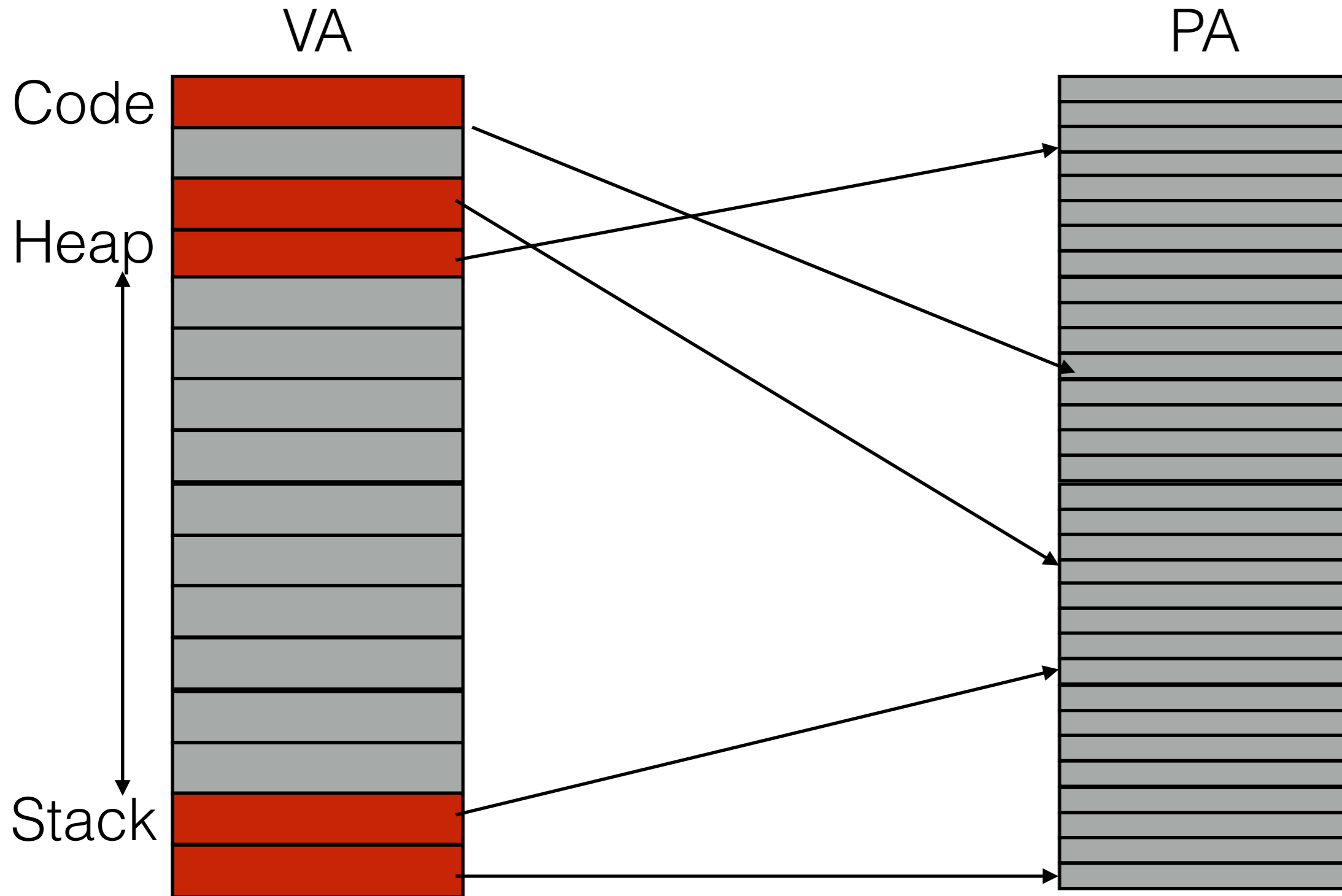
# Reducing Memory Overheads of Paging

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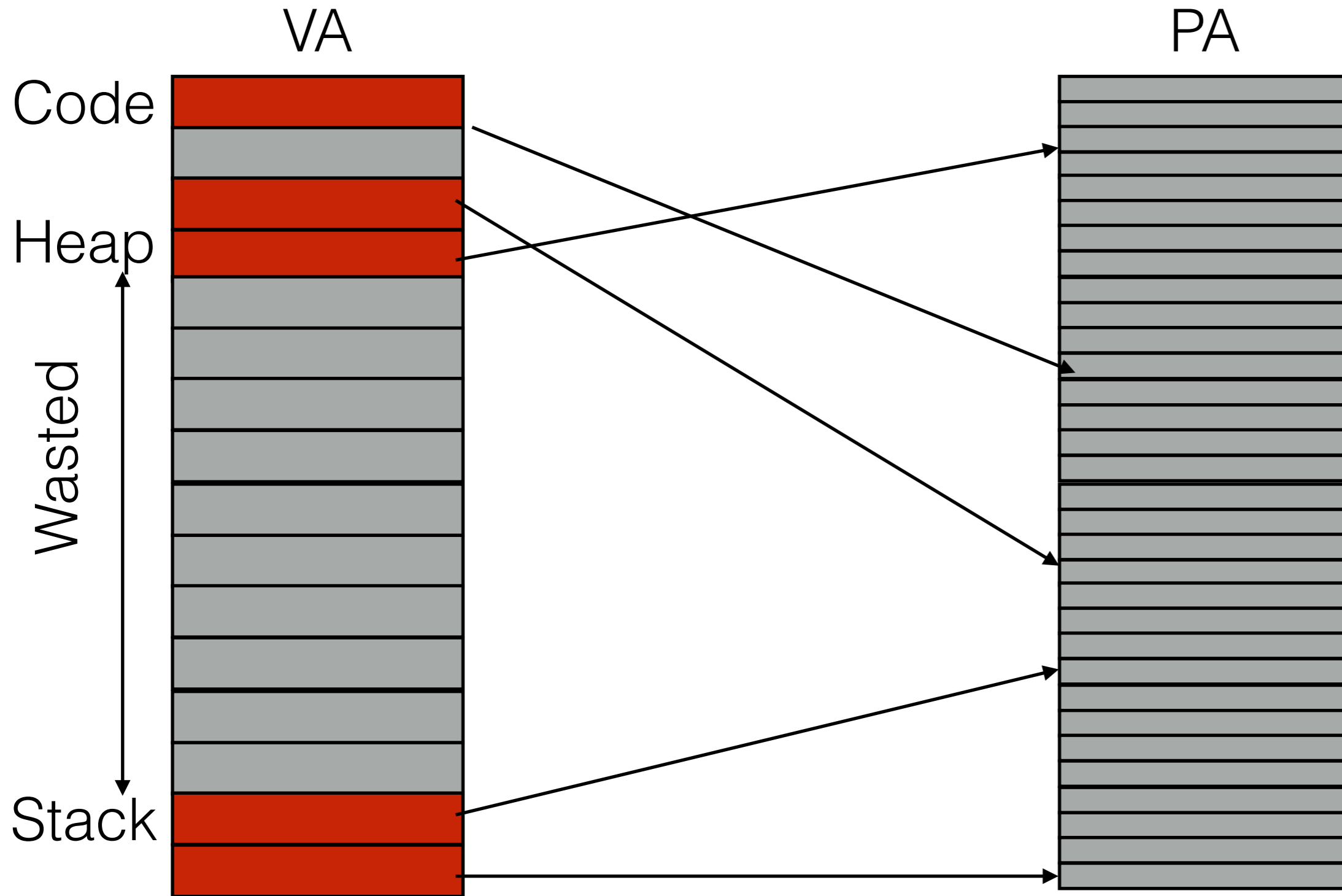
# Reducing Memory Overheads of Paging

---



# Reducing Memory Overheads of Paging

---




# Reducing Memory Overheads of Paging

---

PFN	Valid	...
10	1	..
-	0	
-	0	
-	0	
23	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

# Reducing Memory Overheads of Paging

---



PFN	Valid	...
10	1	..
-	0	
-	0	
-	0	
23	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

# Reducing Memory Overheads of Paging

---

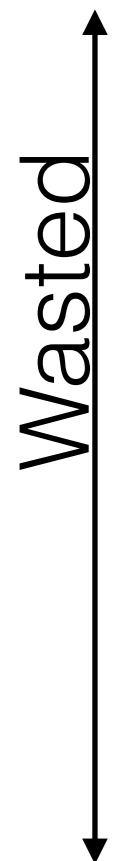
PFN	Valid	...
10	1	..
-	0	
-	0	
-	0	
23	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

Wasted

# Reducing Memory Overheads of Paging

---

Wasted



PFN	Valid	...
10	1	..
-	0	
-	0	
-	0	
23	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

# Reducing Memory Overheads of Paging

PFN	Valid	...
10	1	..
-	0	
-	0	
-	0	
23	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

Linear Page Table

Wasted





# Reducing Memory Overheads of Paging

PFN	Valid	...
10	1	..
-	0	
-	0	
-	0	
23	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

Linear Page Table

Wasted



# Reducing Memory Overheads of Paging

PFN	Valid	...
10	1	..
-	0	
-	0	
-	0	
23	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

Wasted



Linear Page Table

Lookup =  $O(1)$

# Reducing Memory Overheads of Paging

PFN	Valid	...
10	1	..
-	0	
-	0	
-	0	
23	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

Wasted



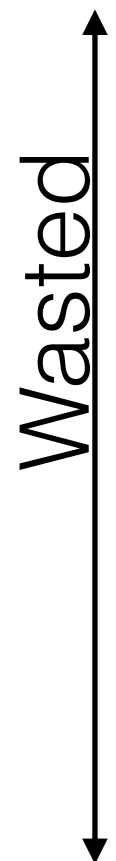
Linear Page Table

Lookup =  $O(1)$   
Space =  $16 * \text{Size}$

# Reducing Memory Overheads of Paging

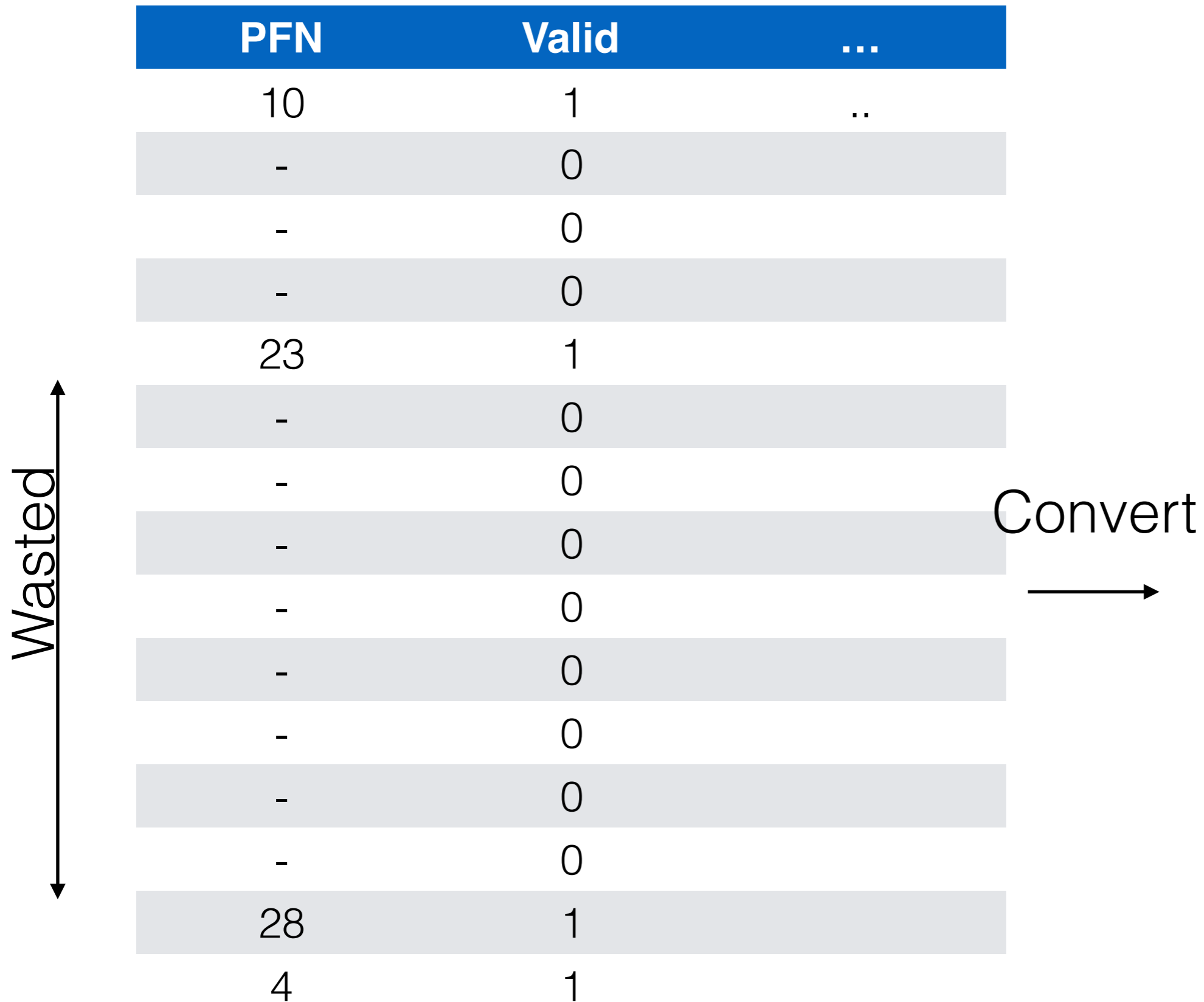
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Wasted

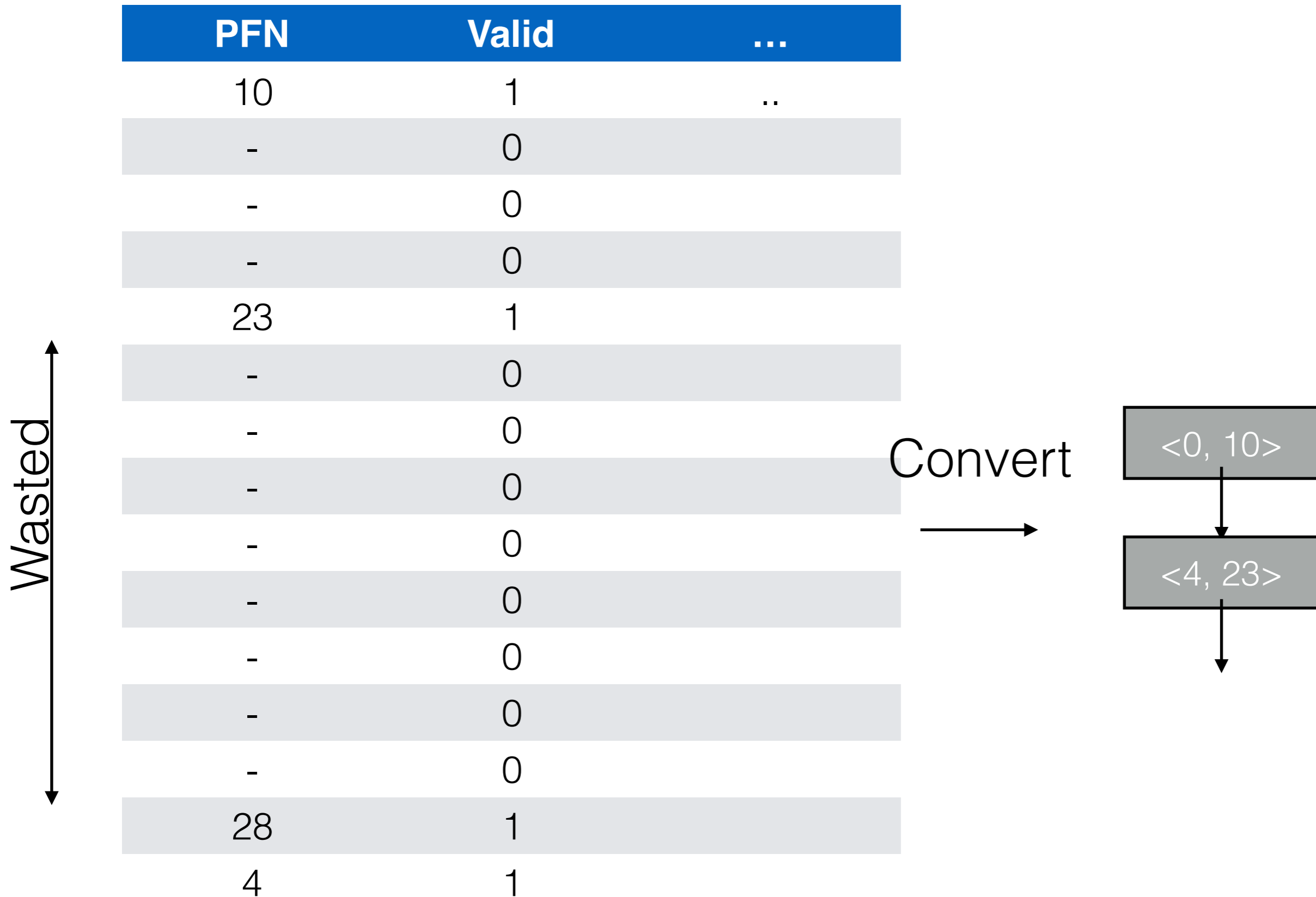


PFN	Valid	...
10	1	..
-	0	
-	0	
-	0	
23	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

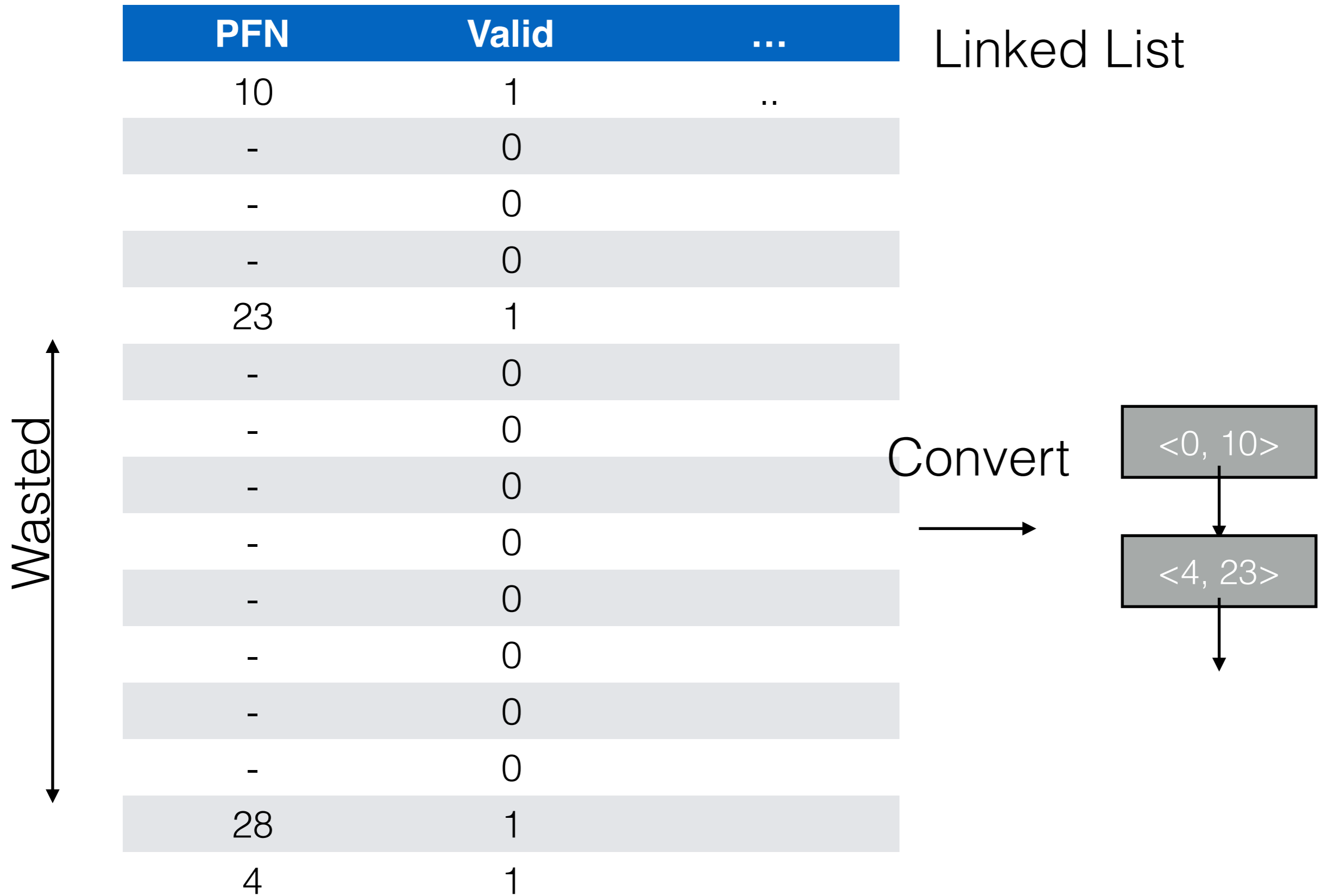
# Reducing Memory Overheads of Paging



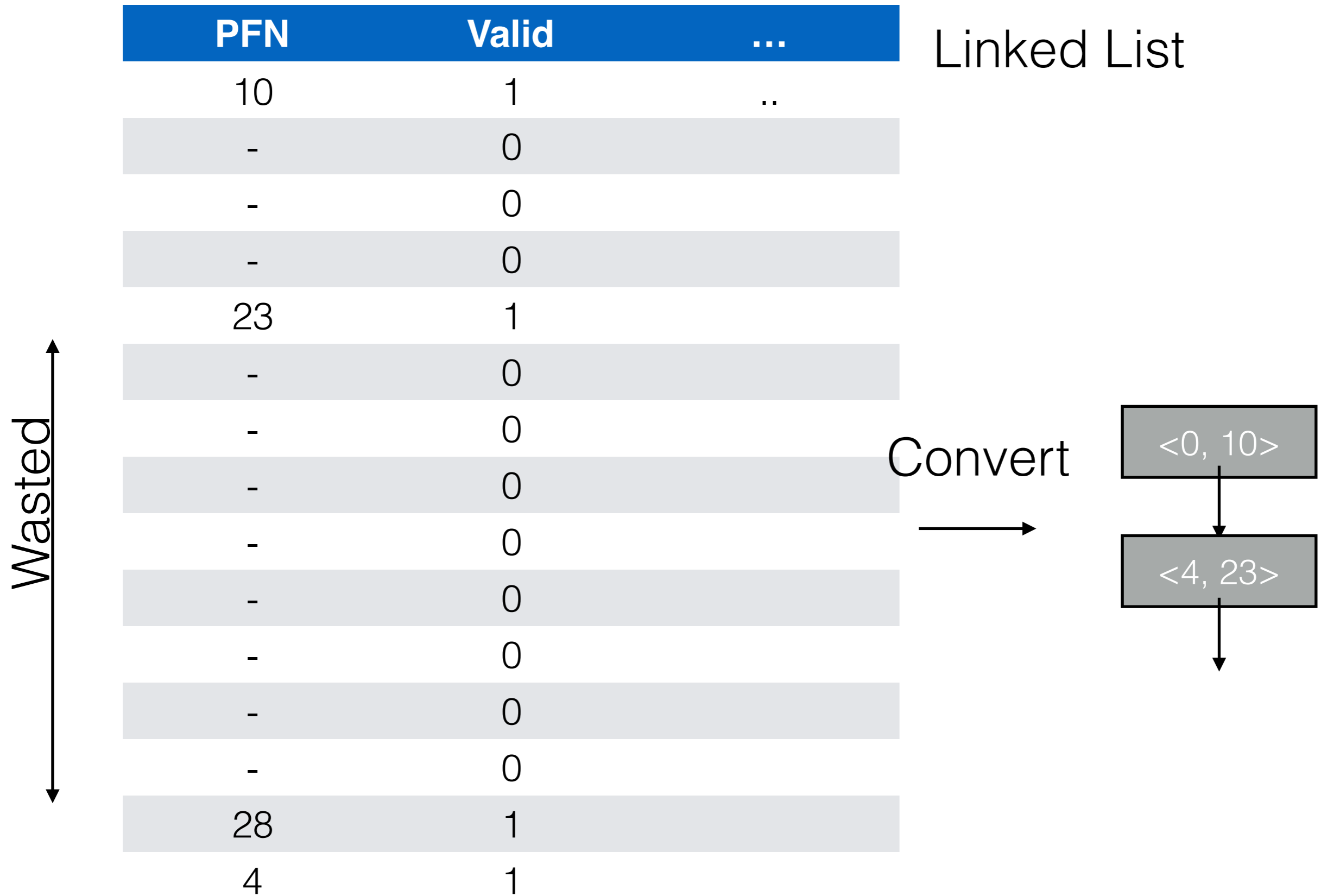
# Reducing Memory Overheads of Paging



# Reducing Memory Overheads of Paging



# Reducing Memory Overheads of Paging





# Reducing Memory Overheads of Paging

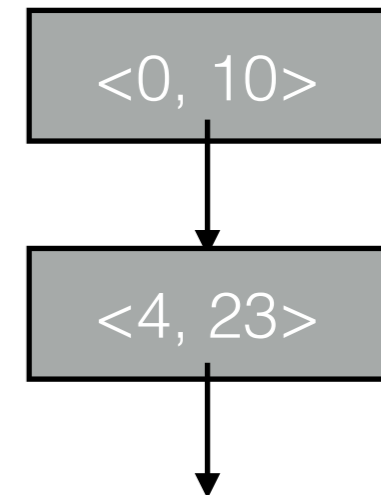
PFN	Valid	...
10	1	..
-	0	
-	0	
-	0	
23	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

Linked List

Lookup =  $O(n)$  for  $n$

Wasted

Convert



# Reducing Memory Overheads of Paging

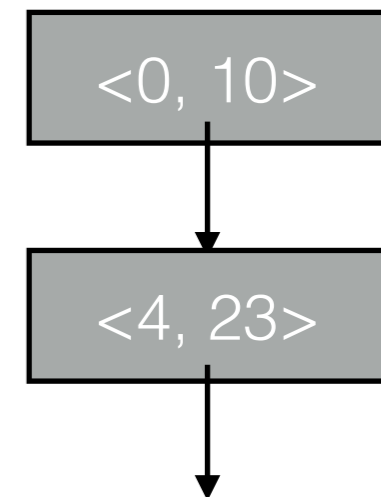
PFN	Valid	...
10	1	..
-	0	
-	0	
-	0	
23	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

Wasted

Linked List

Lookup =  $O(n)$  for  $n$  valid pages ( $n \ll 16$ )

Convert



# Reducing Memory Overheads of Paging

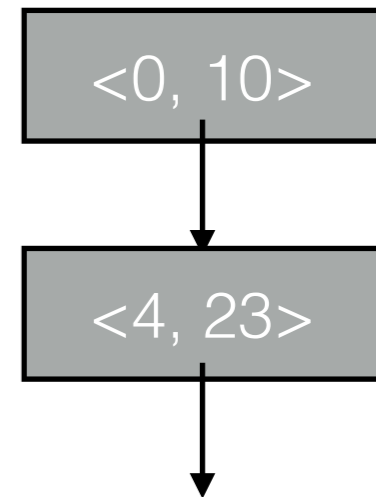
PFN	Valid	...
10	1	..
-	0	
-	0	
-	0	
23	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

Wasted

Linked List

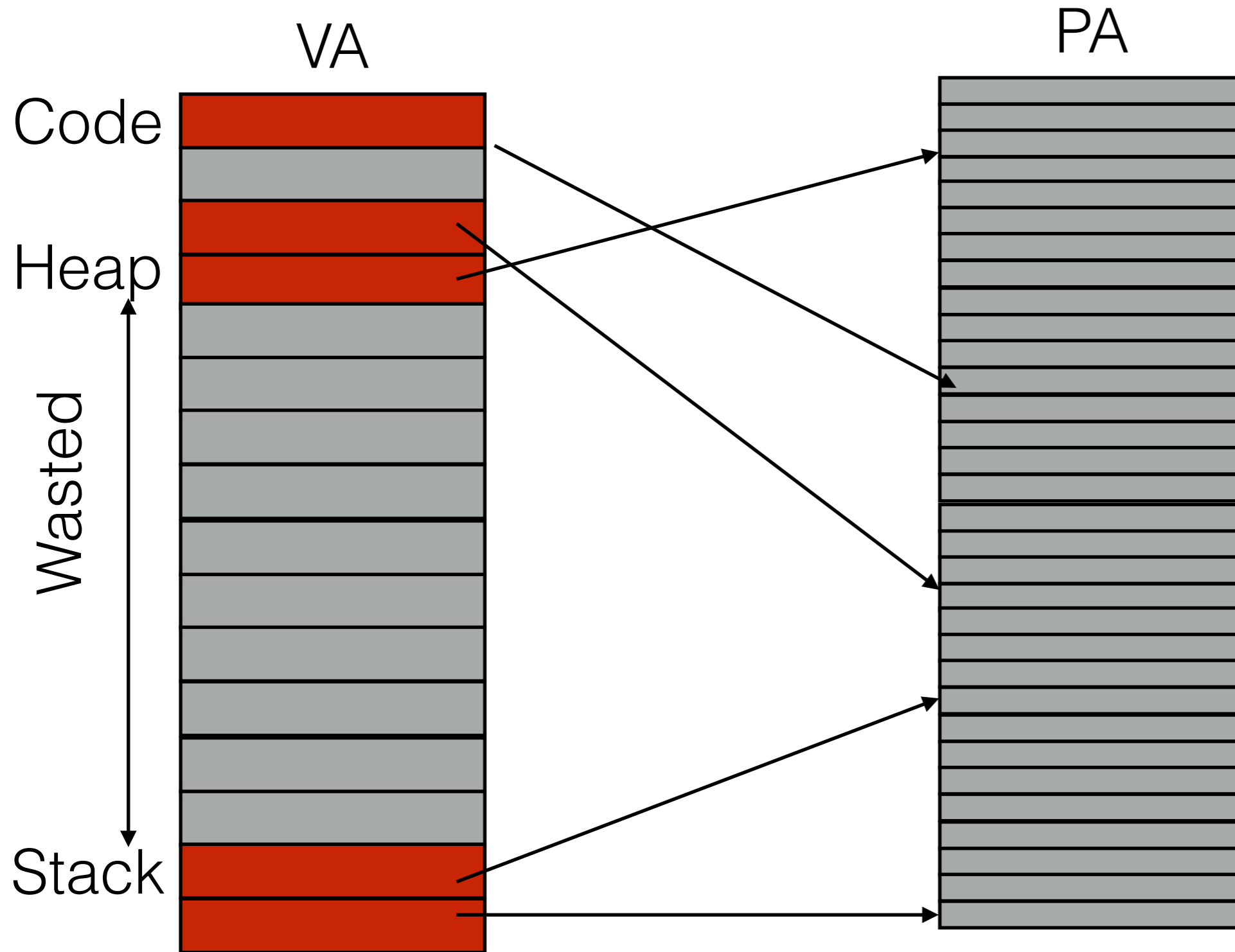
Lookup =  $O(n)$  for  $n$  valid pages ( $n \ll 16$ )  
 Space =  $n * \text{Size}$

Convert



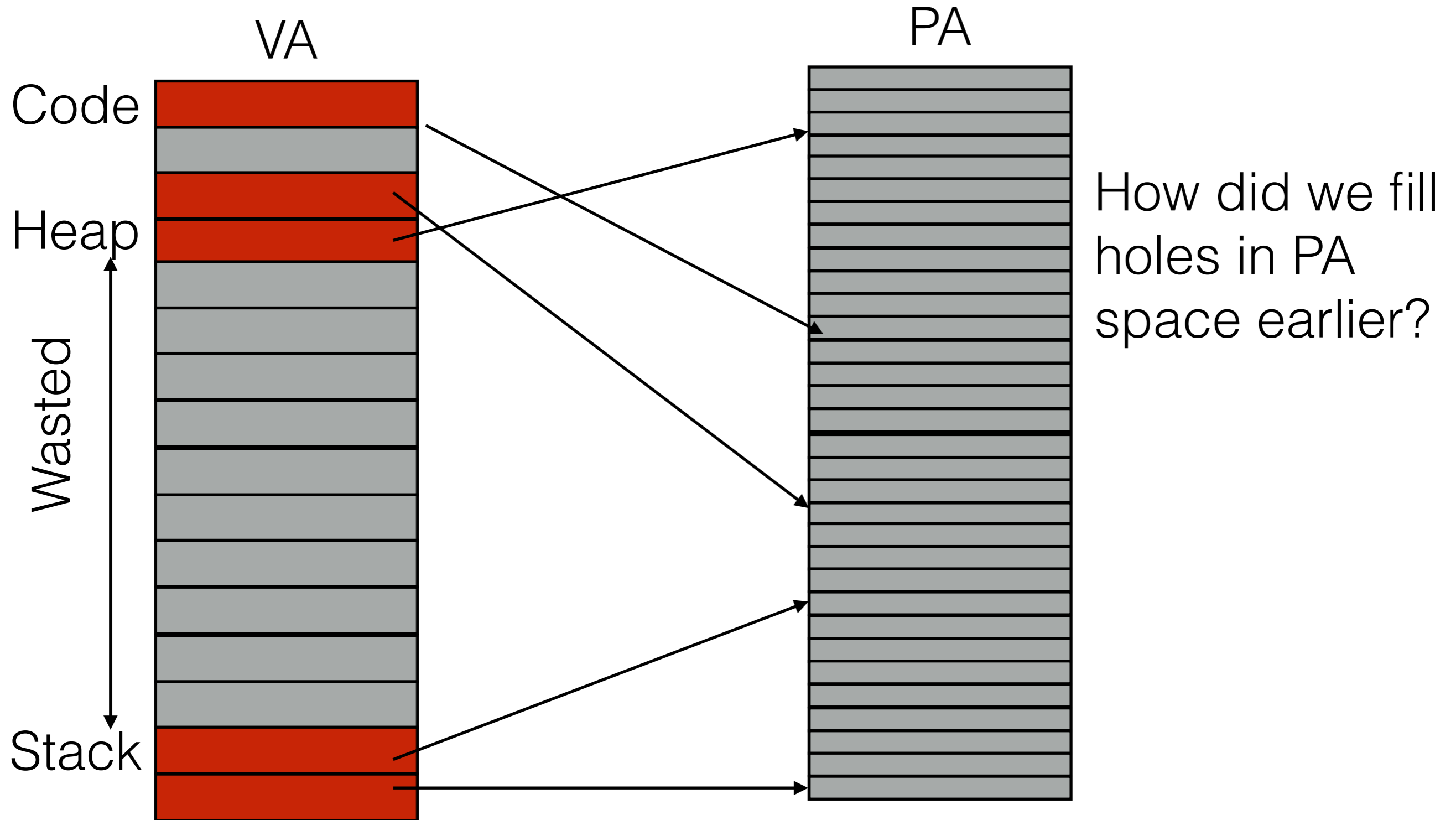
# Reducing Memory Overheads of Paging

---



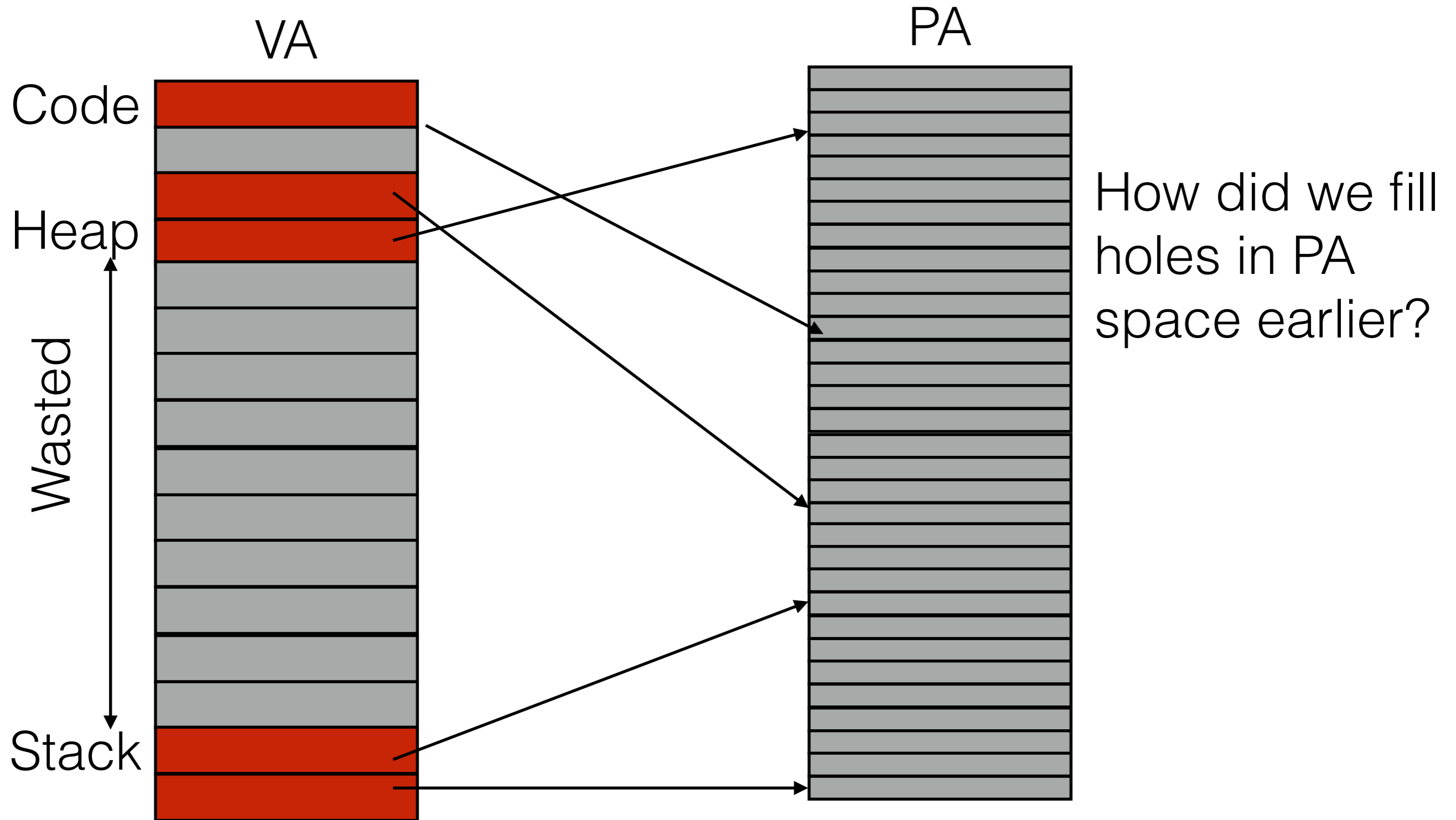
# Reducing Memory Overheads of Paging

---



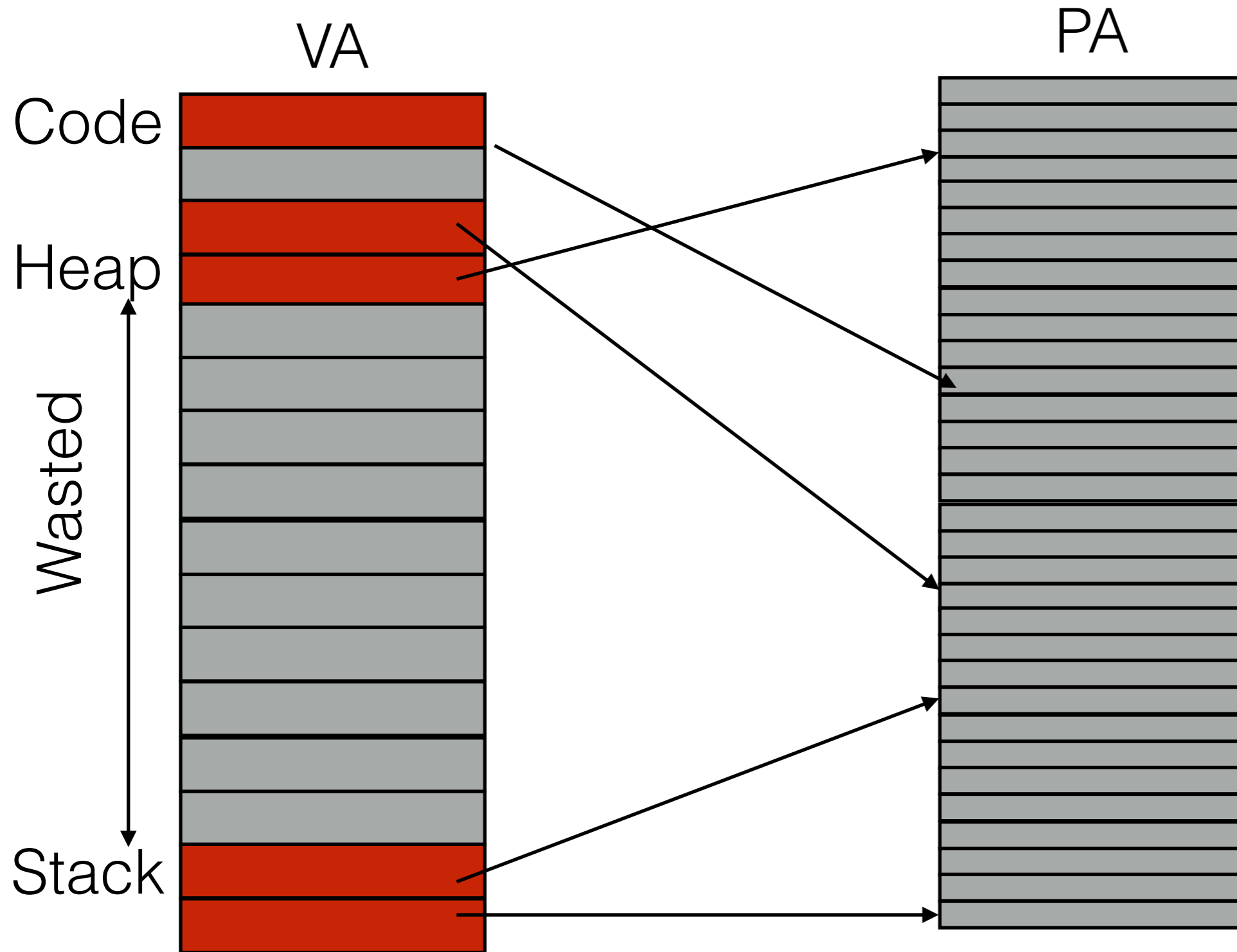
# Reducing Memory Overheads of Paging

---



# Reducing Memory Overheads of Paging

---

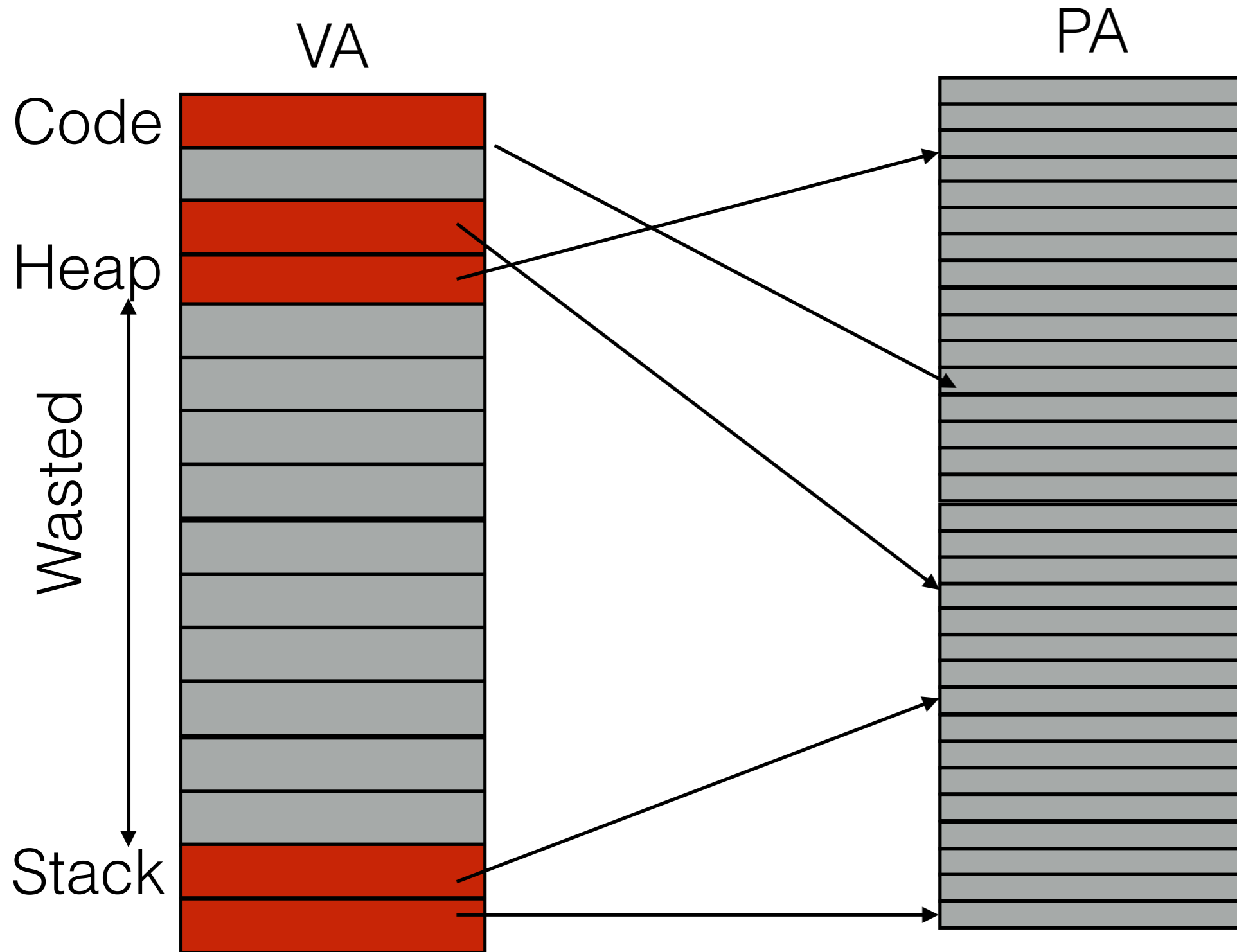


How did we fill holes in PA space earlier?

1. Segmentation

# Reducing Memory Overheads of Paging

---



How did we fill holes in PA space earlier?

1. Segmentation
2. Paging



# Reducing Memory Overheads of Paging - Segmentation + PT

---

# Reducing Memory Overheads of Paging - Segmentation + PT

---

Idea: use different page tables for heap, stack, etc

# Reducing Memory Overheads of Paging - Segmentation + PT

---

Idea: use different page tables for heap, stack, etc

# Reducing Memory Overheads of Paging - Segmentation + PT

---

Idea: use different page tables for heap, stack, etc

- Each PT can be different size

# Reducing Memory Overheads of Paging - Segmentation + PT

---

Idea: use different page tables for heap, stack, etc

- Each PT can be different size
- Each PT has base & bounds

# Reducing Memory Overheads of Paging - Segmentation + PT

---

Idea: use different page tables for heap, stack, etc

- Each PT can be different size
- Each PT has base & bounds
  - Base & Bounds stored in :

# Reducing Memory Overheads of Paging - Segmentation + PT

---

Idea: use different page tables for heap, stack, etc

- Each PT can be different size
- Each PT has base & bounds
  - Base & Bounds stored in :
    - MMU

# Reducing Memory Overheads of Paging - Segmentation + PT

---

Idea: use different page tables for heap, stack, etc

- Each PT can be different size
- Each PT has base & bounds
  - Base & Bounds stored in :
    - MMU
  - What did Base store in regular segmentation?



# Reducing Memory Overheads of Paging - Segmentation + PT

---

Idea: use different page tables for heap, stack, etc

- Each PT can be different size
- Each PT has base & bounds
  - Base & Bounds stored in :
    - MMU
  - What did Base store in regular segmentation?
    - PA where segment resided

# Reducing Memory Overheads of Paging - Segmentation + PT

---

Idea: use different page tables for heap, stack, etc

- Each PT can be different size
- Each PT has base & bounds
  - Base & Bounds stored in :
    - MMU
  - What did Base store in regular segmentation?
    - PA where segment resided
- What would Base refer here?

# Reducing Memory Overheads of Paging - Segmentation + PT

---

Idea: use different page tables for heap, stack, etc

- Each PT can be different size
- Each PT has base & bounds
  - Base & Bounds stored in :
    - MMU
  - What did Base store in regular segmentation?
    - PA where segment resided
  - What would Base refer here?
    - PA of PT for segment

# Reducing Memory Overheads of Paging - Segmentation + PT

---

Idea: use different page tables for heap, stack, etc

- Each PT can be different size
- Each PT has base & bounds
  - Base & Bounds stored in :
    - MMU
  - What did Base store in regular segmentation?
    - PA where segment resided
  - What would Base refer here?
    - PA of PT for segment
  - What would Bounds refer to here?

# Reducing Memory Overheads of Paging - Segmentation + PT

---

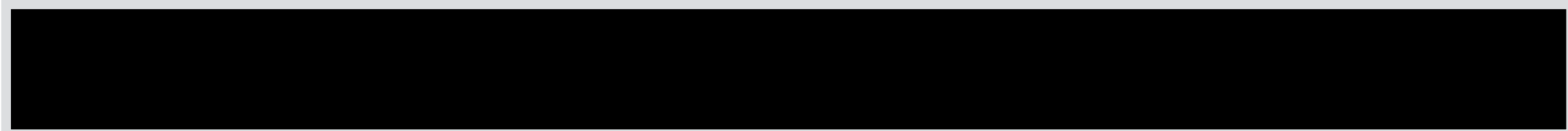
Idea: use different page tables for heap, stack, etc

- Each PT can be different size
- Each PT has base & bounds
  - Base & Bounds stored in :
    - MMU
  - What did Base store in regular segmentation?
    - PA where segment resided
  - What would Base refer here?
    - PA of PT for segment
  - What would Bounds refer to here?
    - Number of valid pages/End of page table

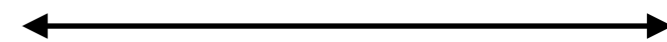
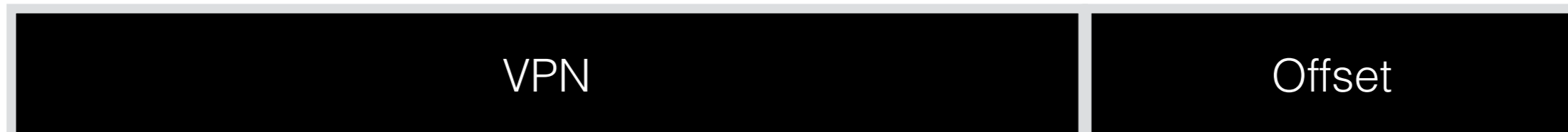
# Reducing Memory Overheads of Paging - Segmentation + PT

---

32 bit VA space

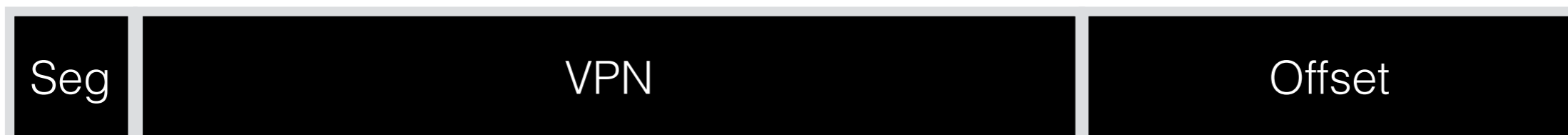


32 bit VA space with 4KB pages



12 bits

32 bit VA space with 4KB pages for 4 segments



2 bits

# Reducing Memory Overheads of Paging - Segmentation + PT

---

PFN	Valid	...
10	1	..
-	0	
-	0	
-	0	
23	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

# Reducing Memory Overheads of Paging - Segmentation + PT

---

PFN	Valid	...
10	1	..
-	0	
-	0	
-	0	
23	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

PFN	Valid	...
10	1	..
..	1	



# Reducing Memory Overheads of Paging - Segmentation + PT

PFN	Valid	...
10	1	..
-	0	
-	0	
-	0	
23	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

Code PT

PFN	Valid	...
10	1	..
..	1	

# Reducing Memory Overheads of Paging - Segmentation + PT

PFN	Valid	...
10	1	..
-	0	
-	0	
-	0	
23	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

Code PT  
Base = 0

PFN	Valid	...
10	1	..
..	1	

# Reducing Memory Overheads of Paging - Segmentation + PT

PFN	Valid	...
10	1	..
-	0	
-	0	
-	0	
23	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

Code PT  
Base = 0  
Bounds = 2

PFN	Valid	...
10	1	..
..	1	

# Reducing Memory Overheads of Paging - Segmentation + PT

PFN	Valid	...
10	1	..
-	0	
-	0	
-	0	
23	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

Code PT  
Base = 0  
Bounds = 2

PFN	Valid	...
10	1	..
..	1	

PFN	Valid	...
23	1	..
..	1	

# Reducing Memory Overheads of Paging - Segmentation + PT

PFN	Valid	...
10	1	..
-	0	
-	0	
-	0	
23	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

Code PT  
Base = 0  
Bounds = 2

PFN	Valid	...
10	1	..
..	1	

Heap PT

PFN	Valid	...
23	1	..
..	1	

# Reducing Memory Overheads of Paging - Segmentation + PT

PFN	Valid	...
10	1	..
-	0	
-	0	
-	0	
23	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

Code PT  
Base = 0  
Bounds = 2

PFN	Valid	...
10	1	..
..	1	

Heap PT  
Base = 4

PFN	Valid	...
23	1	..
..	1	

# Reducing Memory Overheads of Paging - Segmentation + PT

PFN	Valid	...
10	1	..
-	0	
-	0	
-	0	
23	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

Code PT  
Base = 0  
Bounds = 2

PFN	Valid	...
10	1	..
..	1	

Heap PT  
Base = 4  
Bounds = 2

PFN	Valid	...
23	1	..
..	1	

# Reducing Memory Overheads of Paging - Segmentation + PT

PFN	Valid	...
10	1	..
-	0	
-	0	
-	0	
23	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

Code PT  
Base = 0  
Bounds = 2

PFN	Valid	...
10	1	..
..	1	

Heap PT  
Base = 4  
Bounds = 2

PFN	Valid	...
23	1	..
..	1	

Stack PT



# Reducing Memory Overheads of Paging - Segmentation + PT

PFN	Valid	...
10	1	..
-	0	
-	0	
-	0	
23	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

Code PT  
Base = 0  
Bounds = 2

PFN	Valid	...
10	1	..
..	1	

Heap PT  
Base = 4  
Bounds = 2

PFN	Valid	...
23	1	..
..	1	

Stack PT  
Base = ?

# Reducing Memory Overheads of Paging - Segmentation + PT

PFN	Valid	...
10	1	..
-	0	
-	0	
-	0	
23	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

Code PT  
Base = 0  
Bounds = 2

PFN	Valid	...
10	1	..
..	1	

Heap PT  
Base = 4  
Bounds = 2

PFN	Valid	...
23	1	..
..	1	

Stack PT  
Base = ?  
Bounds = ?

# Reducing Memory Overheads of Paging - Segmentation + PT

---

# Reducing Memory Overheads of Paging - Segmentation + PT

---

# Reducing Memory Overheads of Paging - Segmentation + PT

---

- Pros:

# Reducing Memory Overheads of Paging - Segmentation + PT

---

- Pros:
  - Leads to memory saving (Large gaps between segments)

# Reducing Memory Overheads of Paging - Segmentation + PT

---

- Pros:
  - Leads to memory saving (Large gaps between segments)
- Cons:

# Reducing Memory Overheads of Paging - Segmentation + PT

---

- Pros:
  - Leads to memory saving (Large gaps between segments)
- Cons:
  - Uses segmentation



# Reducing Memory Overheads of Paging - Segmentation + PT

---

- Pros:
  - Leads to memory saving (Large gaps between segments)
- Cons:
  - Uses segmentation
    - Assumes certain usage pattern of address space

# Reducing Memory Overheads of Paging - Segmentation + PT

---

- Pros:
  - Leads to memory saving (Large gaps between segments)
- Cons:
  - Uses segmentation
    - Assumes certain usage pattern of address space
    - Sparsely used segments (sub-segment internal fragmentation) have same space waste issue

# Reducing Memory Overheads of Paging - Segmentation + PT

---

- Pros:
  - Leads to memory saving (Large gaps between segments)
- Cons:
  - Uses segmentation
    - Assumes certain usage pattern of address space
    - Sparsely used segments (sub-segment internal fragmentation) have same space waste issue
      - How to address this?

# Reducing Memory Overheads of Paging - Segmentation + PT

---

- Pros:
  - Leads to memory saving (Large gaps between segments)
- Cons:
  - Uses segmentation
    - Assumes certain usage pattern of address space
    - Sparsely used segments (sub-segment internal fragmentation) have same space waste issue
      - How to address this?
        - **LinkedList! Getting complex now.**

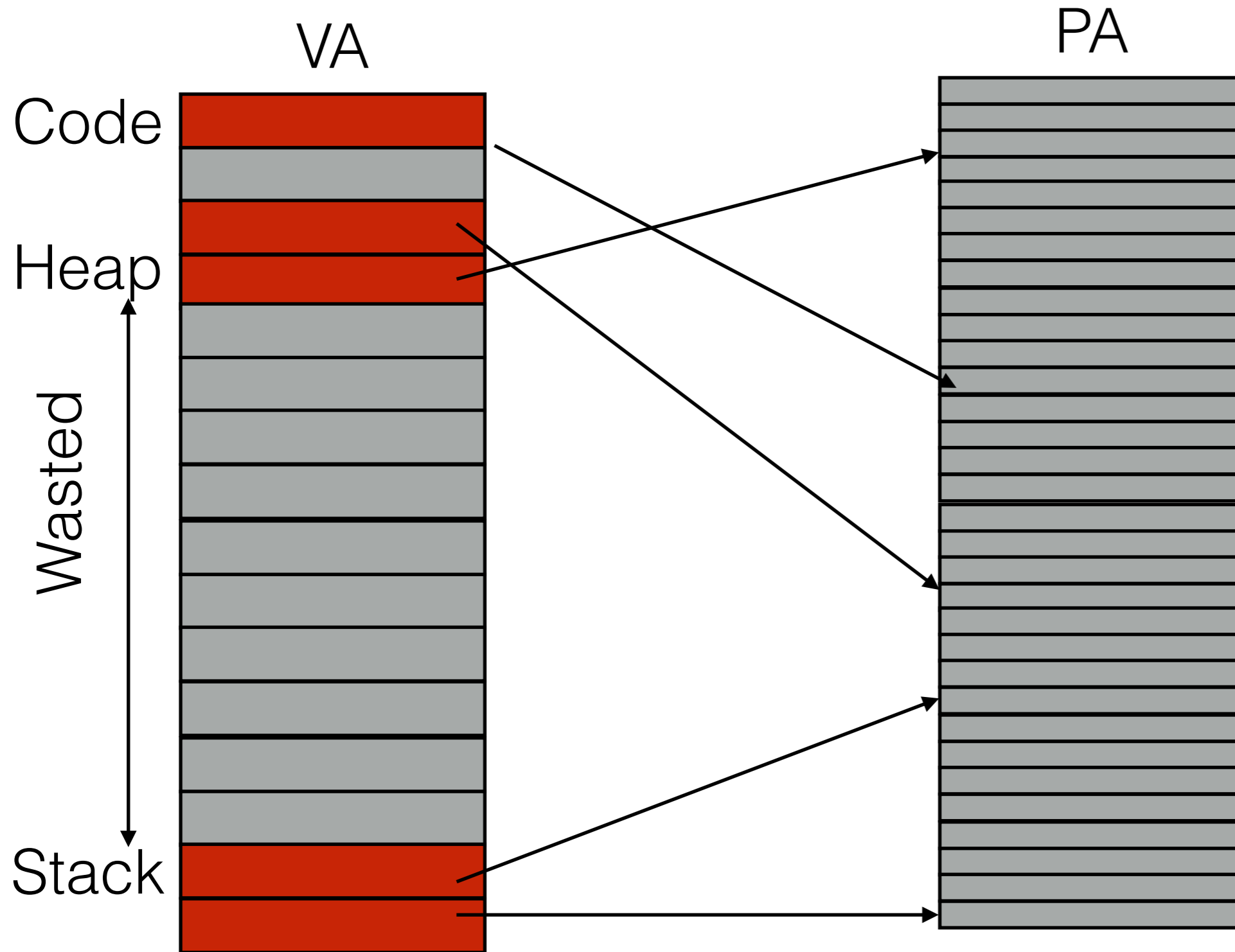
# Reducing Memory Overheads of Paging - Segmentation + PT

---

- Pros:
  - Leads to memory saving (Large gaps between segments)
- Cons:
  - Uses segmentation
    - Assumes certain usage pattern of address space
    - Sparsely used segments (sub-segment internal fragmentation) have same space waste issue
      - How to address this?
        - LinkedList! Getting complex now.
      - **Variable size page tables —> Can lead to fragmentation**

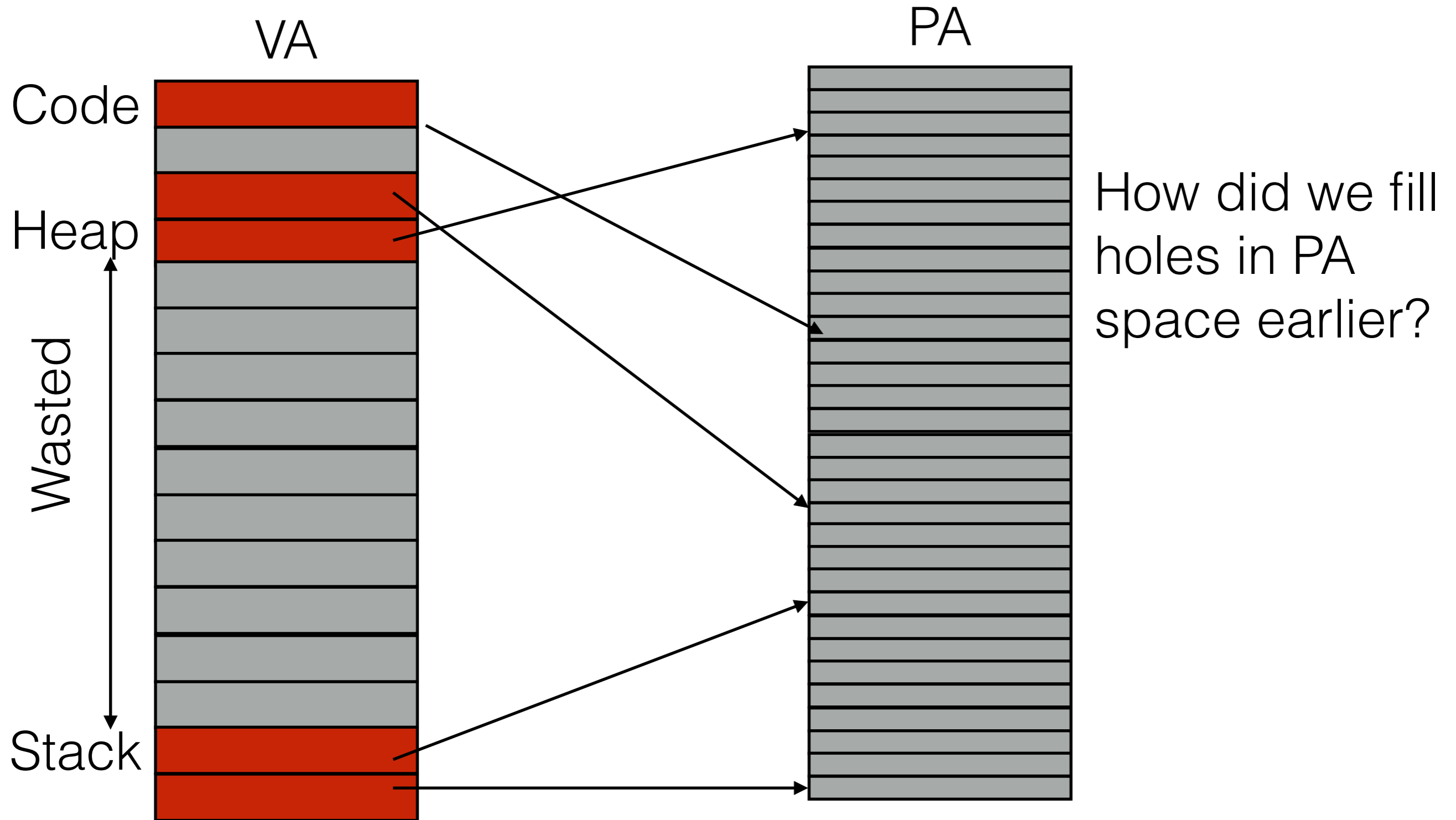
# Reducing Memory Overheads of Paging

---



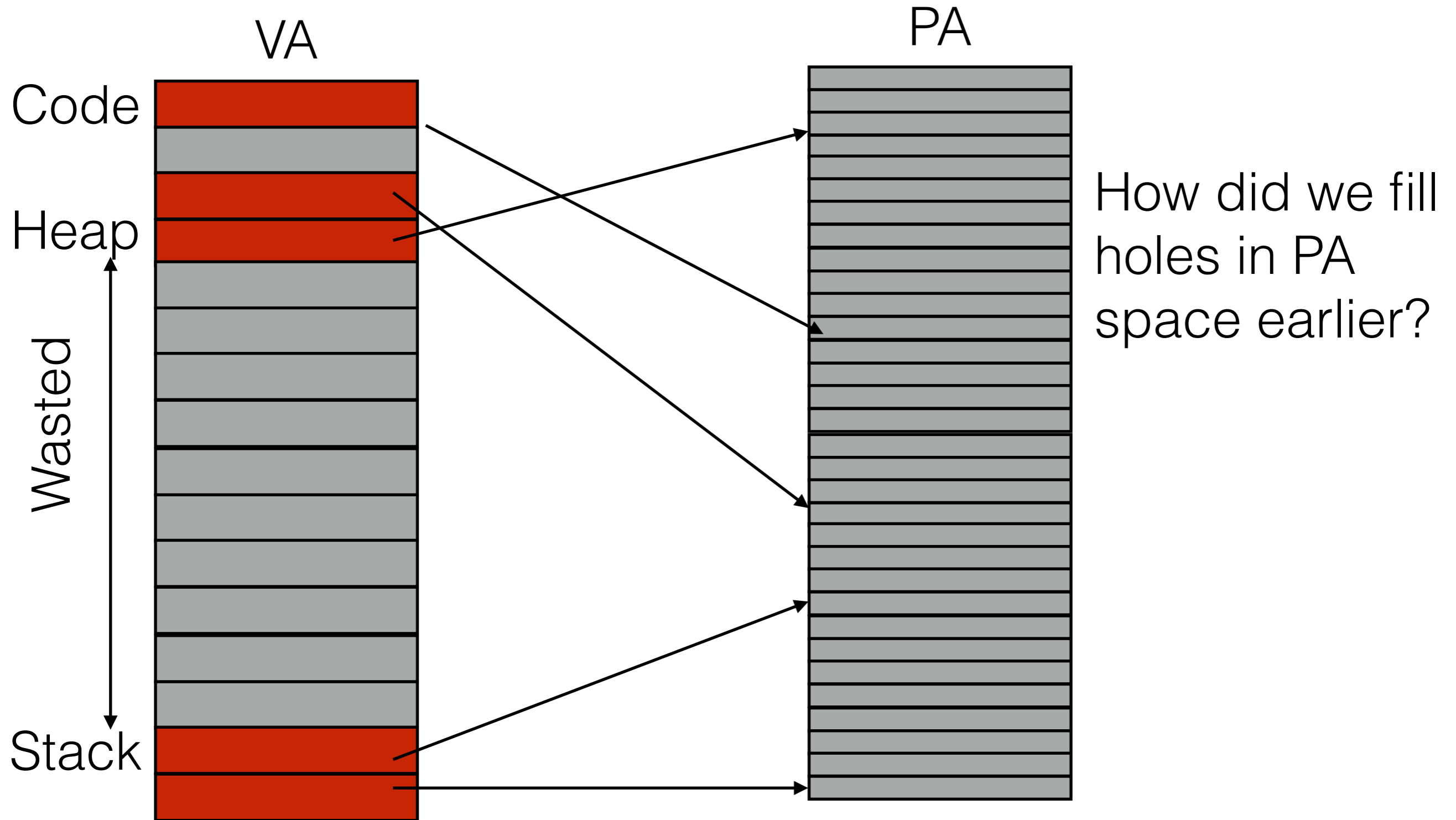
# Reducing Memory Overheads of Paging

---



# Reducing Memory Overheads of Paging

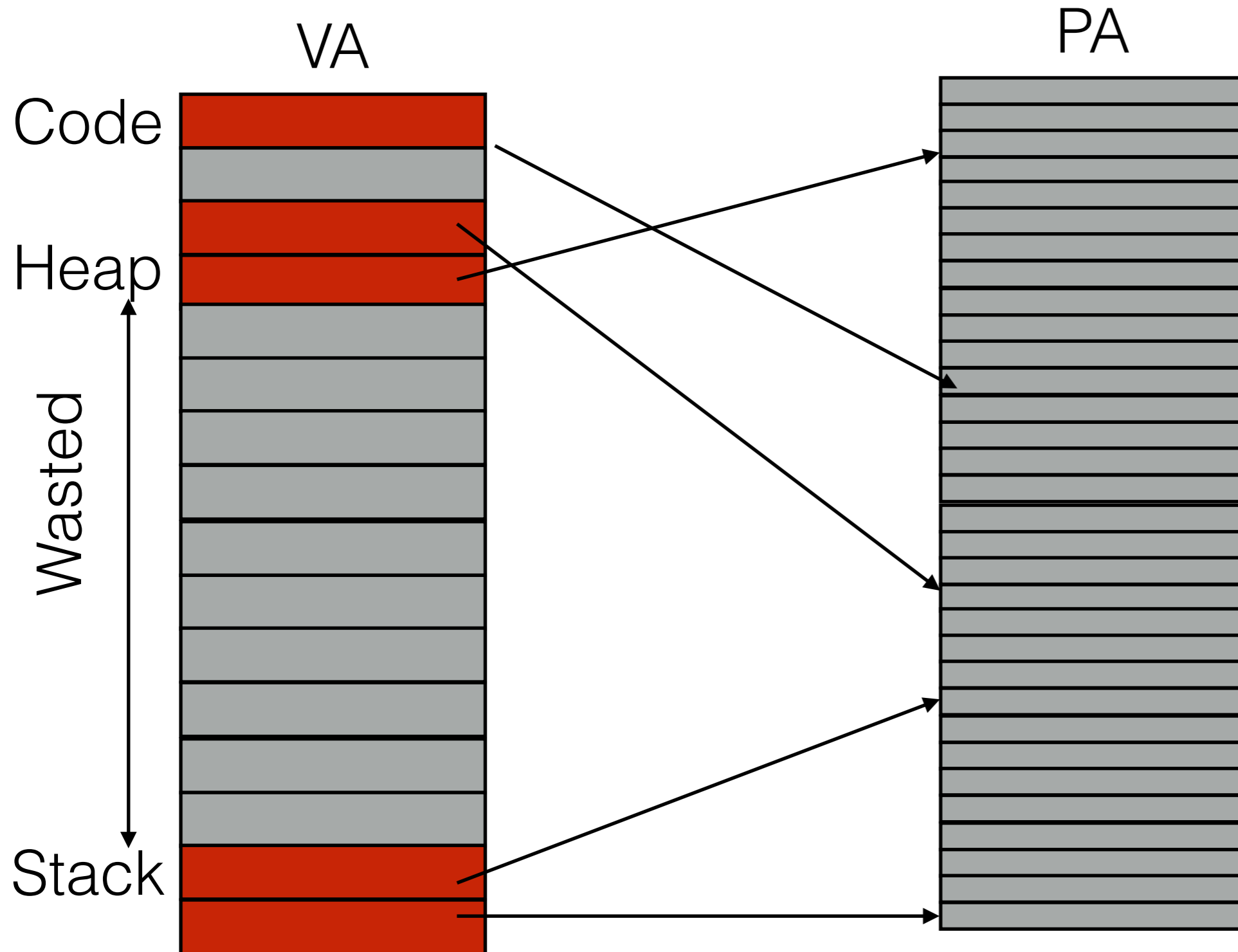
---





# Reducing Memory Overheads of Paging

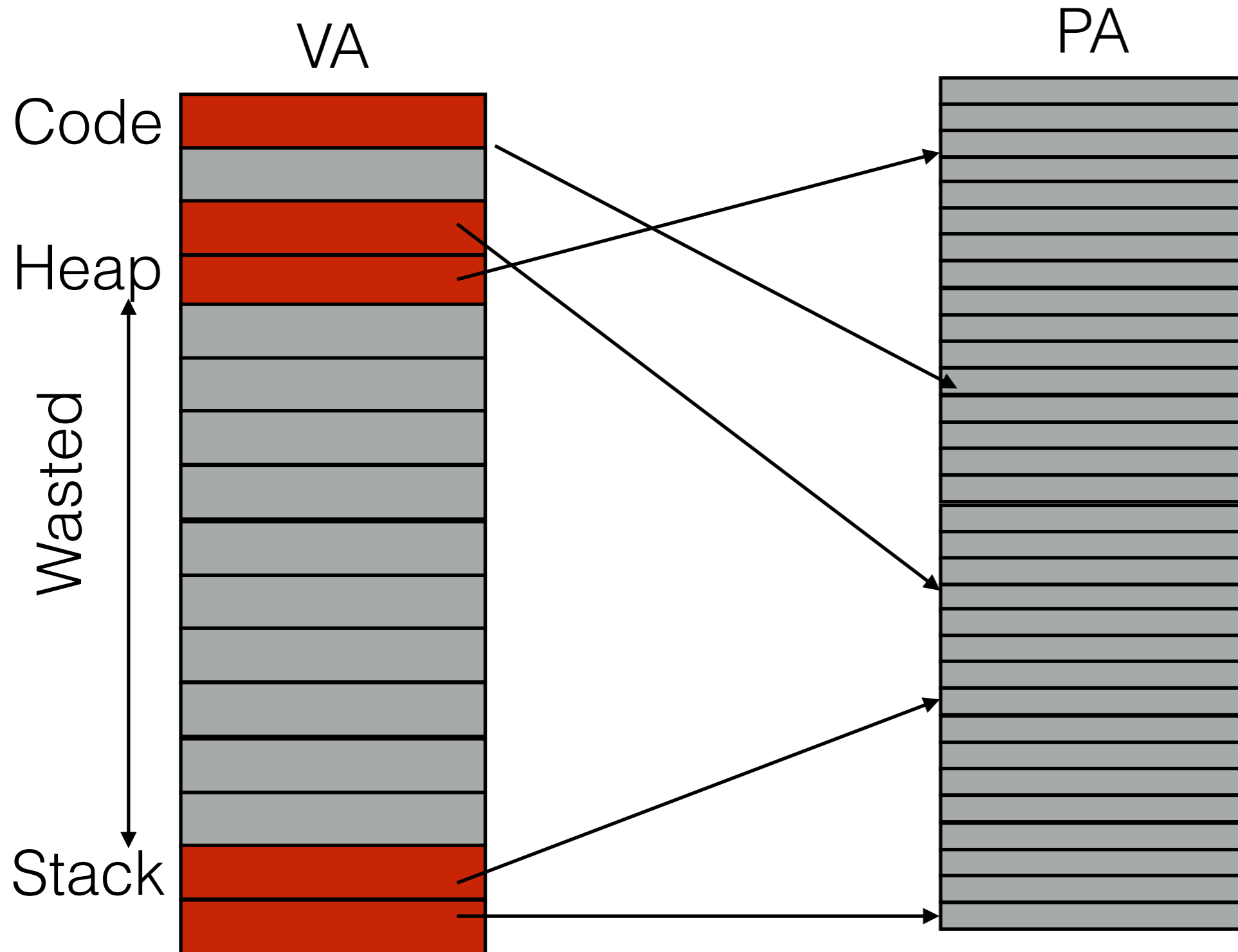
---



How did we fill holes in PA space earlier?

1. Segmentation

# Reducing Memory Overheads of Paging



How did we fill holes in PA space earlier?

1. Segmentation
- 2. Paging**

# Reducing Memory Overheads of Paging - PT + PT (Multi-level Paging)

---

# Reducing Memory Overheads of Paging - PT + PT (Multi-level Paging)

---

Idea: break PT itself into pages

# Reducing Memory Overheads of Paging - PT + PT (Multi-level Paging)

---

Idea: break PT itself into pages

# Reducing Memory Overheads of Paging - PT + PT (Multi-level Paging)

---

Idea: break PT itself into pages

- A Page Directory refers to pieces

# Reducing Memory Overheads of Paging - PT + PT (Multi-level Paging)

---

Idea: break PT itself into pages

- A Page Directory refers to pieces
- Only have pieces with  $>0$  valid entries

# Reducing Memory Overheads of Paging - Segmentation + PT

---

	PFN	Valid	...
PFN = 200	10	1	..
	-	0	
	-	0	
	23	1	
PFN = 201	-	1	
	-	0	
	-	0	
	-	0	
PFN = 202	-	0	
	-	0	
	-	0	
	-	0	
PFN = 203	-	0	
	-	0	
	28	1	
	4	1	

Page Directory  
Entry (PDE)

**Total entries = 16**



# Reducing Memory Overheads of Paging - Segmentation + PT

---

	PFN	Valid	...
PFN = 200	10	1	..
	-	0	
	-	0	
	23	1	
PFN = 201	-	1	
	-	0	
	-	0	
	-	0	
PFN = 202	-	0	
	-	0	
	-	0	
	-	0	
PFN = 203	-	0	
	-	0	
	28	1	
	4	1	

Page Directory  
Entry (PDE)

**Total entries = 16**

# Reducing Memory Overheads of Paging - Segmentation + PT

PFN = 200

PFN	Valid	...
10	1	..
-	0	
-	0	
23	1	
-	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

Page Directory Entry (PDE)

PFN	Valid	...
10	1	..
-	0	
-	0	
23	1	...

**Total entries = 16**

# Reducing Memory Overheads of Paging - Segmentation + PT

PFN = 200

PFN	Valid	...
10	1	..
-	0	
-	0	
23	1	
-	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

Page Directory Entry (PDE)

PFN	Valid	...
10	1	..
-	0	
-	0	
23	1	...

PFN	Valid	...
-	0	..
-	0	
-	0	
-	0	...

**Total entries = 16**

# Reducing Memory Overheads of Paging - Segmentation + PT

PFN = 200

PFN	Valid	...
10	1	..
-	0	
-	0	
23	1	
-	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

PFN = 201

-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	

PFN = 202

-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	

PFN = 203

-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	

Page Directory Entry (PDE)

PFN	Valid	...
10	1	..
-	0	
-	0	
23	1	...

PFN	Valid	...
-	0	..
-	0	
-	0	
-	0	...

PFN	Valid	...
-	0	..
-	0	
-	0	
-	0	...

**Total entries = 16**

# Reducing Memory Overheads of Paging - Segmentation + PT

PFN = 200

PFN	Valid	...
10	1	..
-	0	
-	0	
23	1	
-	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

Page Directory Entry (PDE)

PFN	Valid	...
10	1	..
-	0	
-	0	
23	1	...

PFN	Valid	...
-	0	..
-	0	
-	0	
-	0	...

PFN	Valid	...
-	0	..
-	0	
-	0	
-	0	...

PFN	Valid	...
-	0	..
-	0	
28	1	
4	1	...

**Total entries = 16**

# Reducing Memory Overheads of Paging - Segmentation + PT

PFN = 200

PFN	Valid	...
10	1	..
-	0	
-	0	
23	1	
-	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

Page Directory Entry (PDE)

PFN	Valid	...
201	1	..
202	0	
203	0	
204	1	...

PFN	Valid	...
10	1	..
-	0	
-	0	
23	1	...

PFN	Valid	...
-	0	..
-	0	
-	0	
-	0	...

PFN	Valid	...
-	0	..
-	0	
-	0	
-	0	...

PFN	Valid	...
-	0	..
-	0	
28	1	
4	1	...

**Total entries = 16**

# Reducing Memory Overheads of Paging - Segmentation + PT

PFN = 200

PFN	Valid	...
10	1	..
-	0	
-	0	
23	1	
-	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

Page Directory Entry (PDE)

PFN = 200

PFN	Valid	...
201	1	..
202	0	
203	0	
204	1	...

PFN	Valid	...
10	1	..
-	0	
-	0	
23	1	...

PFN	Valid	...
-	0	..
-	0	
-	0	
-	0	...

PFN	Valid	...
-	0	..
-	0	
-	0	
-	0	...

PFN	Valid	...
-	0	..
-	0	
28	1	
4	1	...

**Total entries = 16**

# Reducing Memory Overheads of Paging - Segmentation + PT

PFN = 200

PFN	Valid	...
10	1	..
-	0	
-	0	
23	1	
-	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

Page Directory Entry (PDE)

PFN = 200

PFN	Valid	...
201	1	..
202	0	
203	0	
204	1	...

PFN = 201

PFN	Valid	...
10	1	..
-	0	
-	0	
23	1	...

PFN	Valid	...
-	0	..
-	0	
-	0	
-	0	...

PFN	Valid	...
-	0	..
-	0	
-	0	
-	0	...

PFN	Valid	...
-	0	..
-	0	
28	1	
4	1	...

**Total entries = 16**



# Reducing Memory Overheads of Paging - Segmentation + PT

PFN = 200

PFN	Valid	...
10	1	..
-	0	
-	0	
23	1	
-	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

PFN = 201

PFN	Valid	...
-	0	..
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	

PFN = 202

PFN	Valid	...
-	0	..
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	

PFN = 203

PFN	Valid	...
-	0	..
-	0	
28	1	
4	1	

**Total entries = 16**

Page Directory Entry (PDE)

PFN = 200

PFN	Valid	...
201	1	..
202	0	
203	0	
204	1	...

PFN = 201

PFN	Valid	...
10	1	..
-	0	
-	0	
23	1	...

PFN = 202

PFN	Valid	...
-	0	..
-	0	
-	0	
-	0	...

PFN	Valid	...
-	0	..
-	0	
-	0	
-	0	...

PFN	Valid	...
-	0	..
-	0	
28	1	
4	1	...

# Reducing Memory Overheads of Paging - Segmentation + PT

PFN = 200

PFN	Valid	...
10	1	..
-	0	
-	0	
23	1	
-	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

PFN = 201

-	0	..
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	

PFN = 202

-	0	..
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	

PFN = 203

-	0	..
-	0	
28	1	
4	1	

**Total entries = 16**

Page Directory Entry (PDE)

PFN = 200

PFN	Valid	...
201	1	..
202	0	
203	0	
204	1	...

PFN = 201

PFN	Valid	...
10	1	..
-	0	
-	0	
23	1	...

PFN = 202

PFN	Valid	...
-	0	..
-	0	
-	0	
-	0	...

PFN = 203

PFN	Valid	...
-	0	..
-	0	
-	0	
-	0	...

PFN	Valid	...
-	0	..
-	0	
28	1	
4	1	...

# Reducing Memory Overheads of Paging - Segmentation + PT

PFN = 200

PFN	Valid	...
10	1	..
-	0	
-	0	
23	1	
-	1	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
-	0	
28	1	
4	1	

PFN = 201

Page Directory Entry (PDE)

PFN = 200

PFN	Valid	...
201	1	..
202	0	
203	0	
204	1	...

PFN = 201

PFN	Valid	...
10	1	..
-	0	
-	0	
23	1	...

PFN = 202

PFN	Valid	...
-	0	..
-	0	
-	0	
-	0	...

PFN = 203

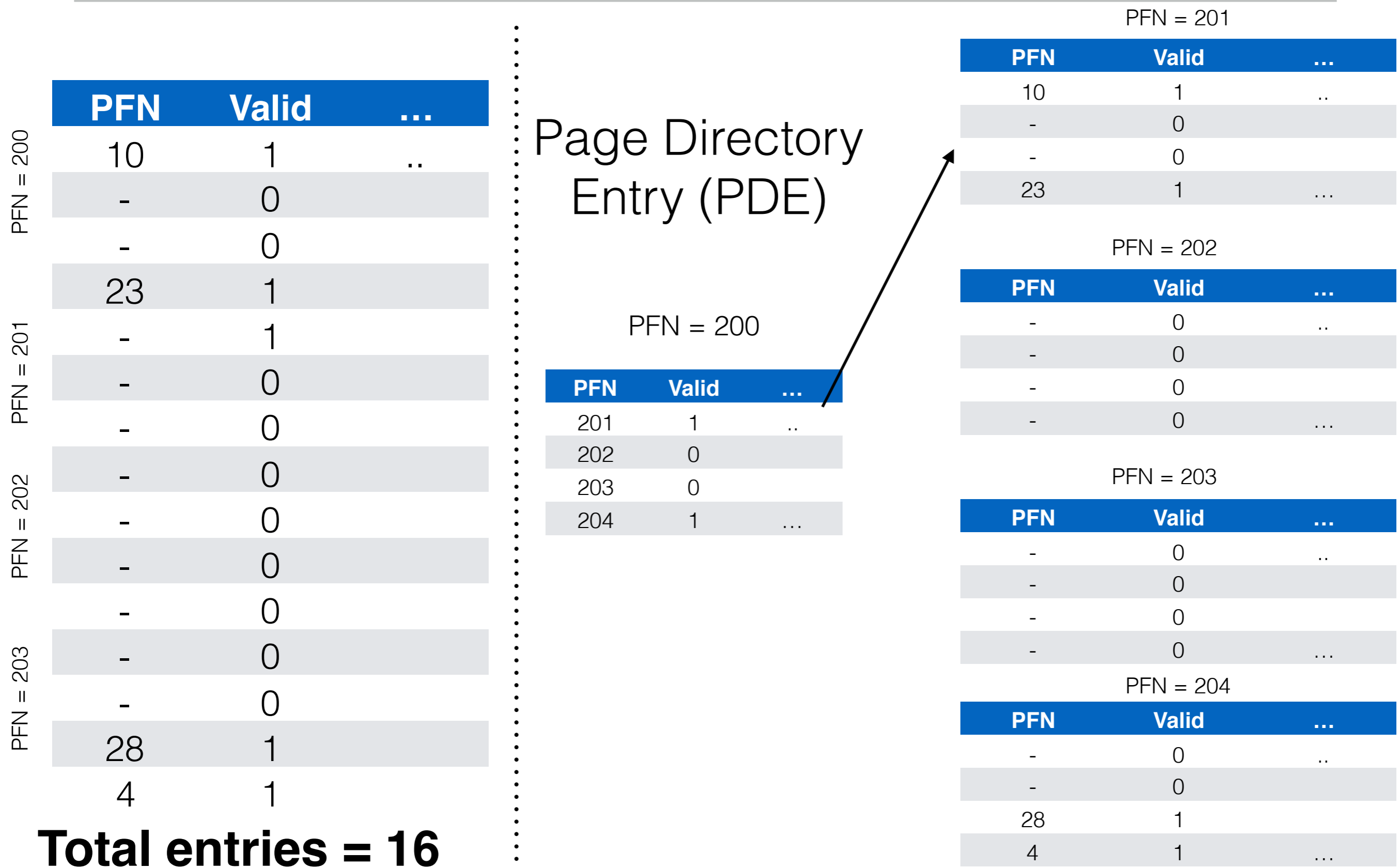
PFN	Valid	...
-	0	..
-	0	
-	0	
-	0	...

PFN = 204

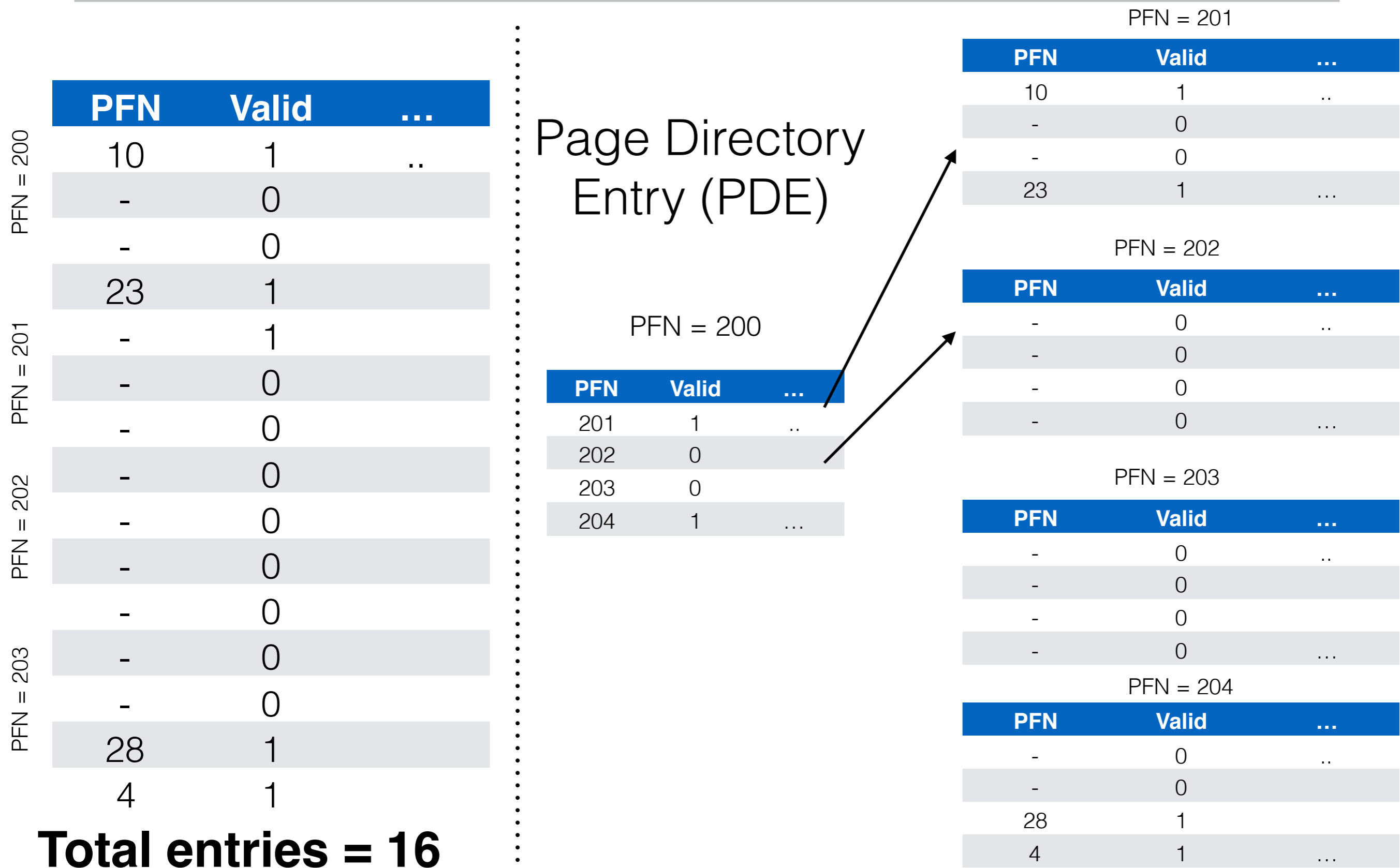
PFN	Valid	...
-	0	..
-	0	
28	1	
4	1	...

**Total entries = 16**

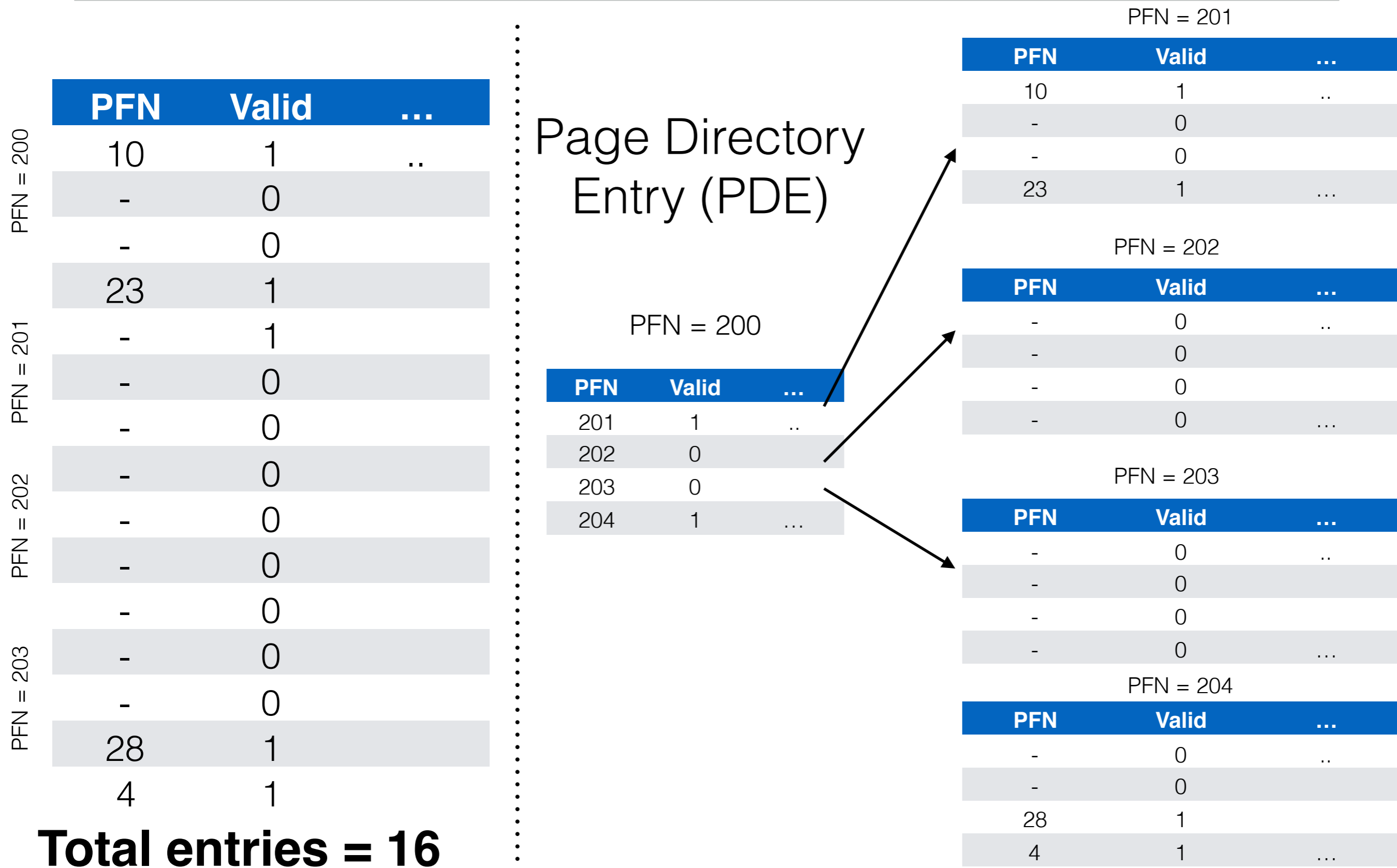
# Reducing Memory Overheads of Paging - Segmentation + PT



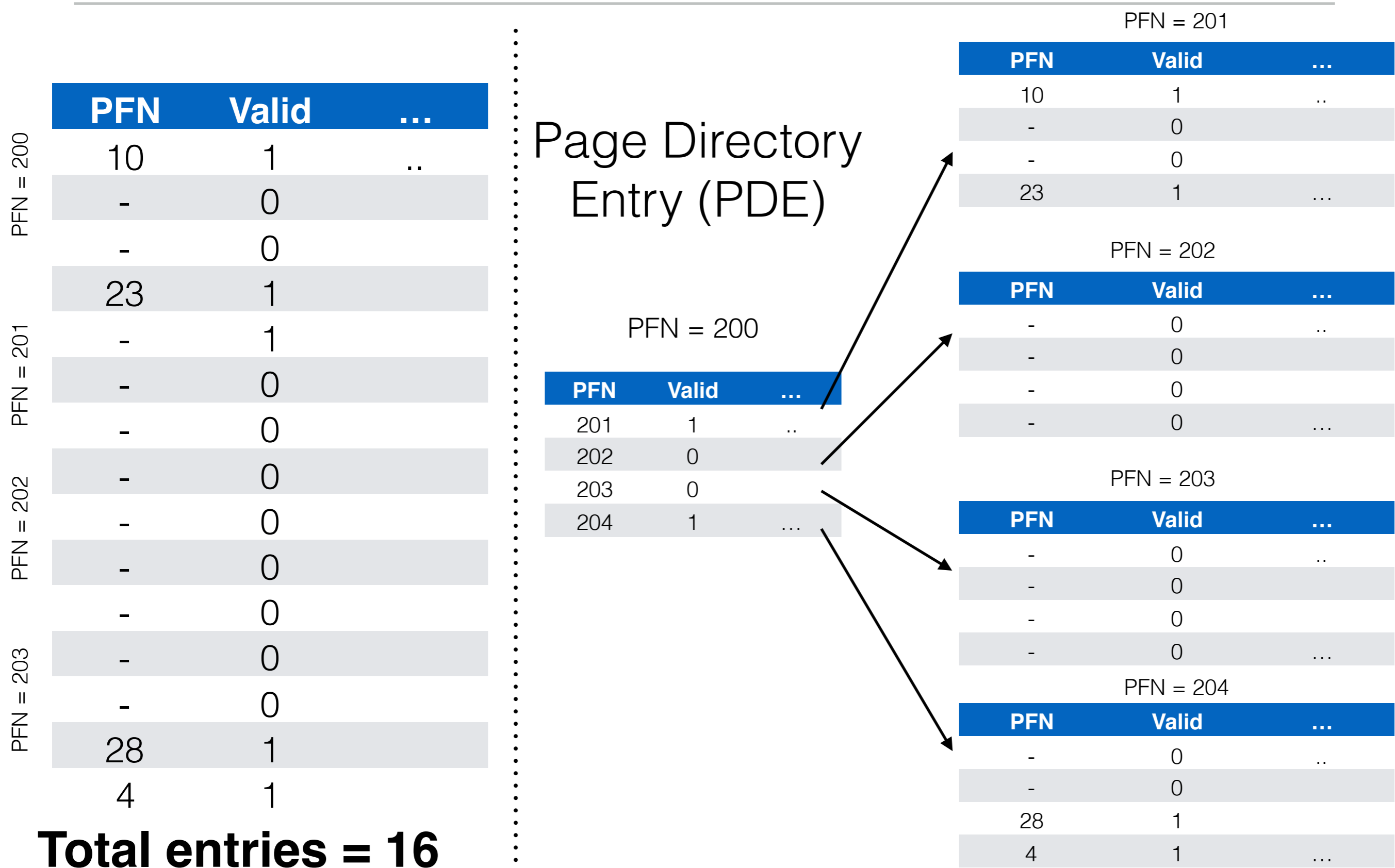
# Reducing Memory Overheads of Paging - Segmentation + PT



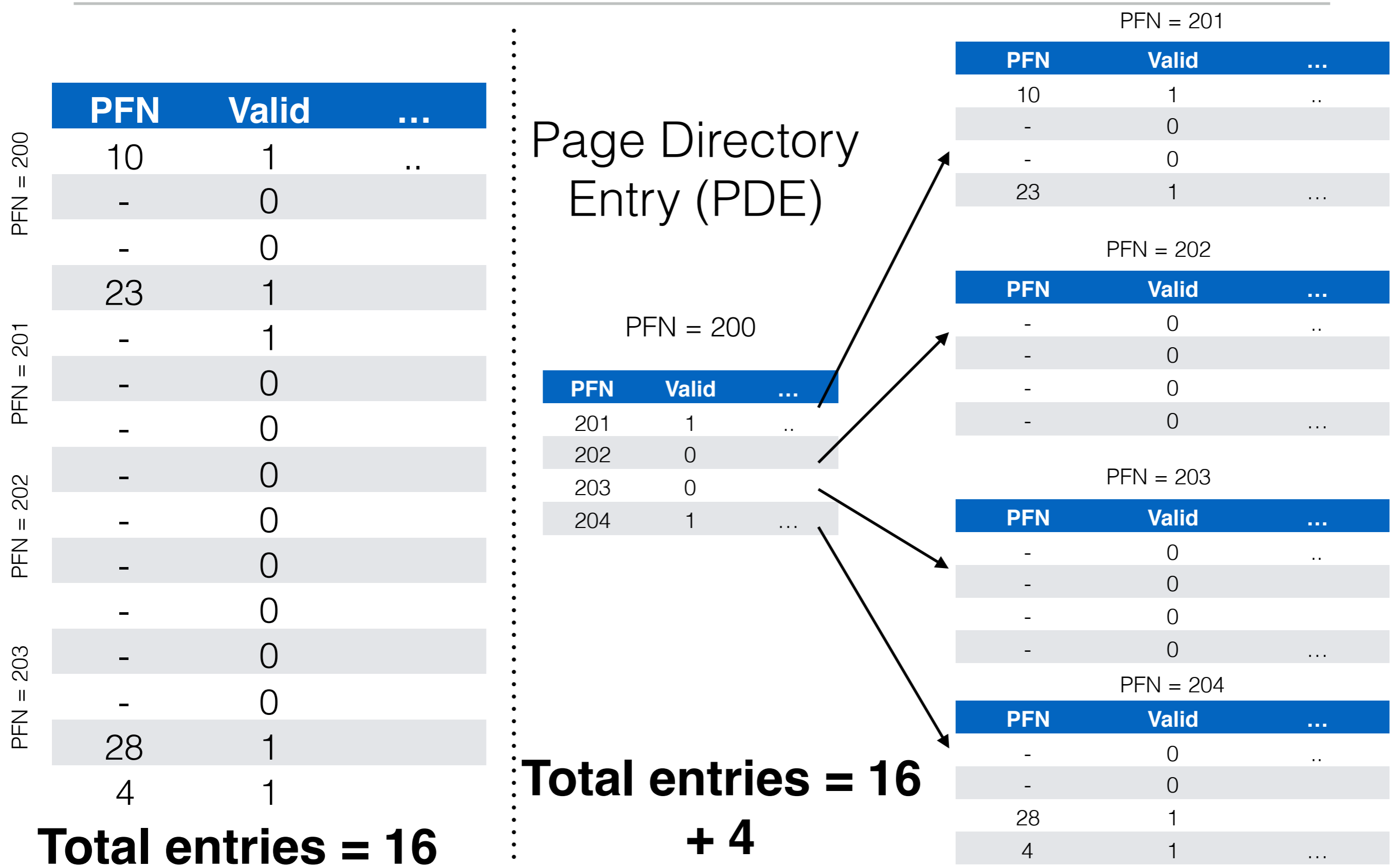
# Reducing Memory Overheads of Paging - Segmentation + PT



# Reducing Memory Overheads of Paging - Segmentation + PT

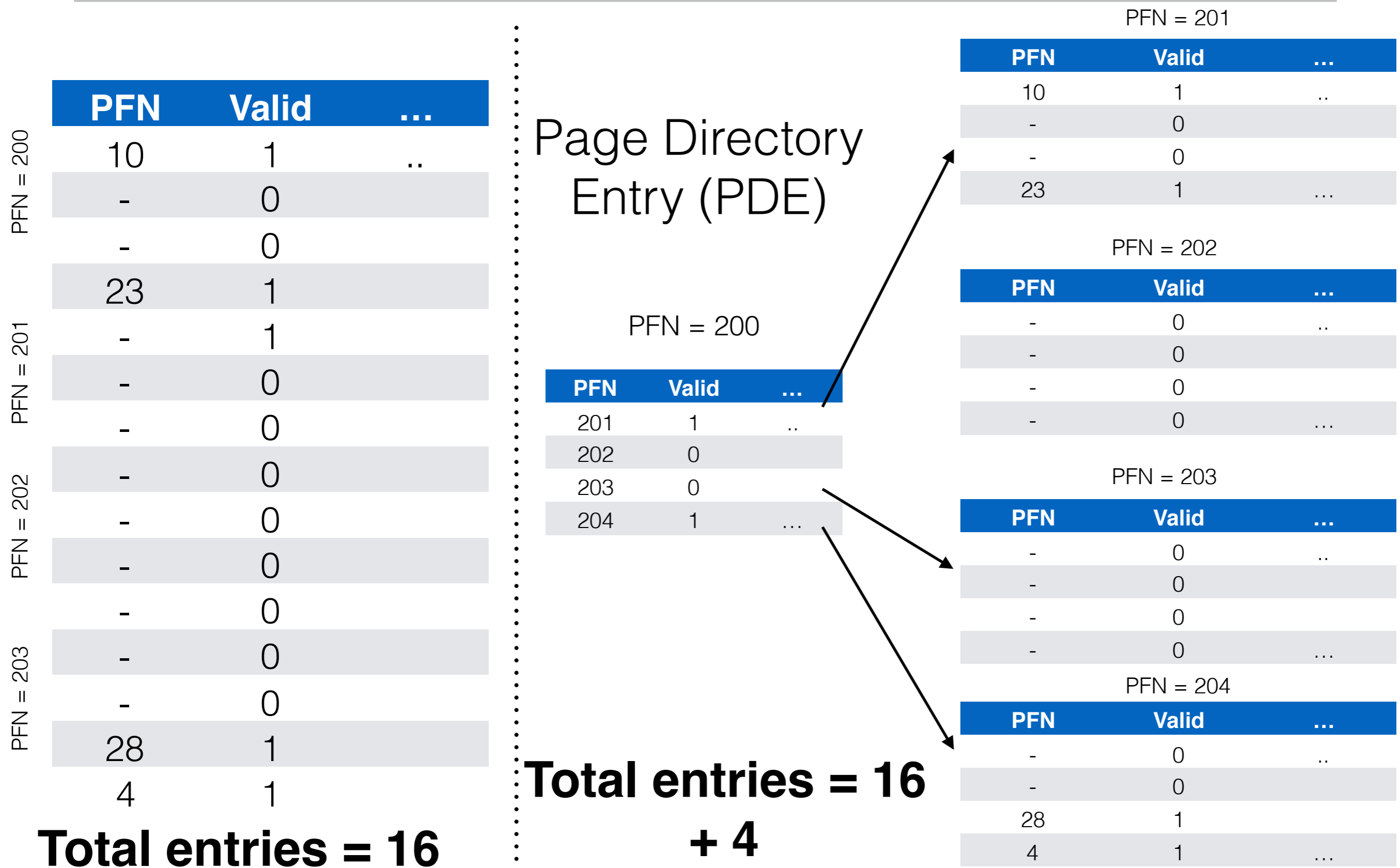


# Reducing Memory Overheads of Paging - Segmentation + PT

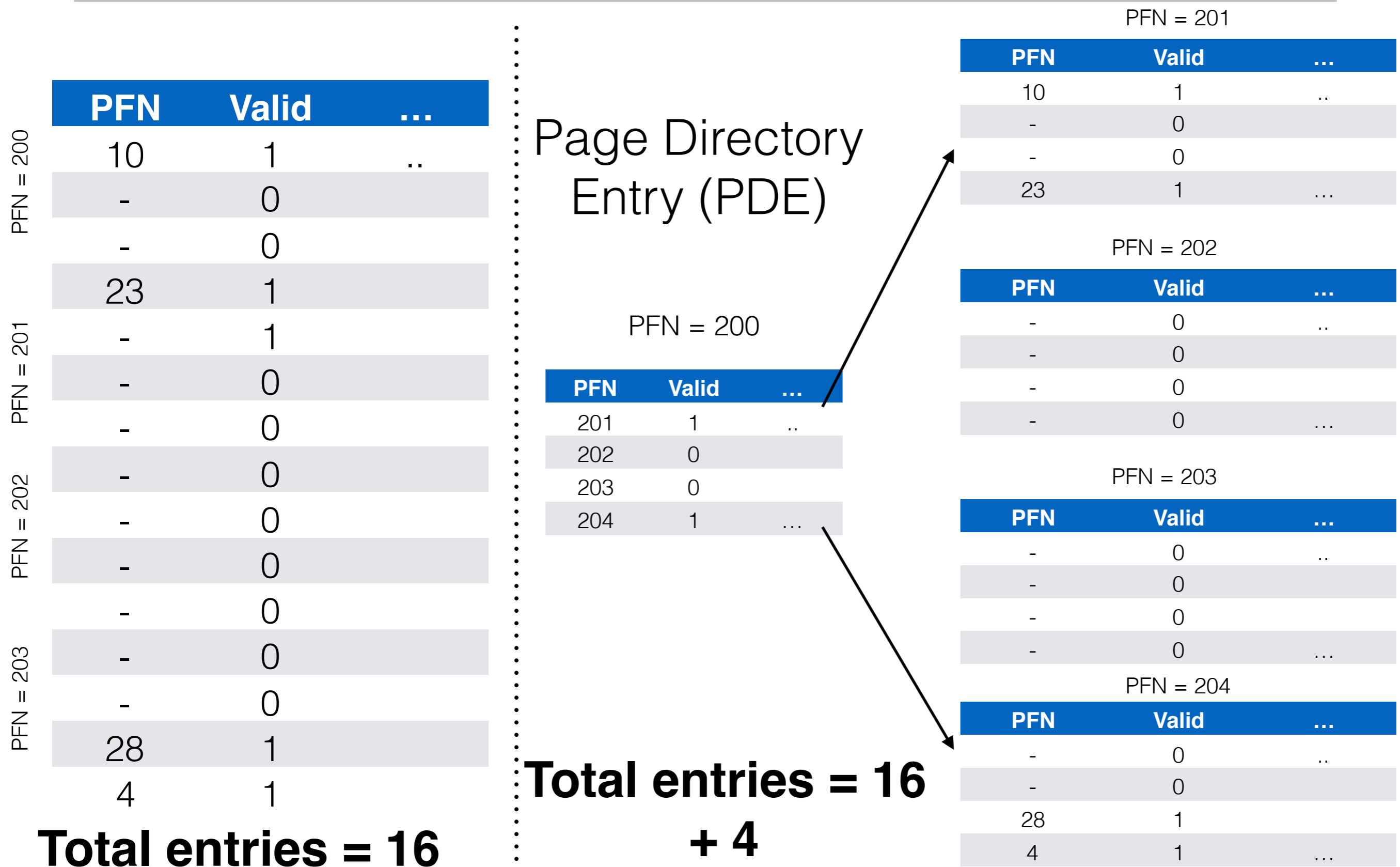




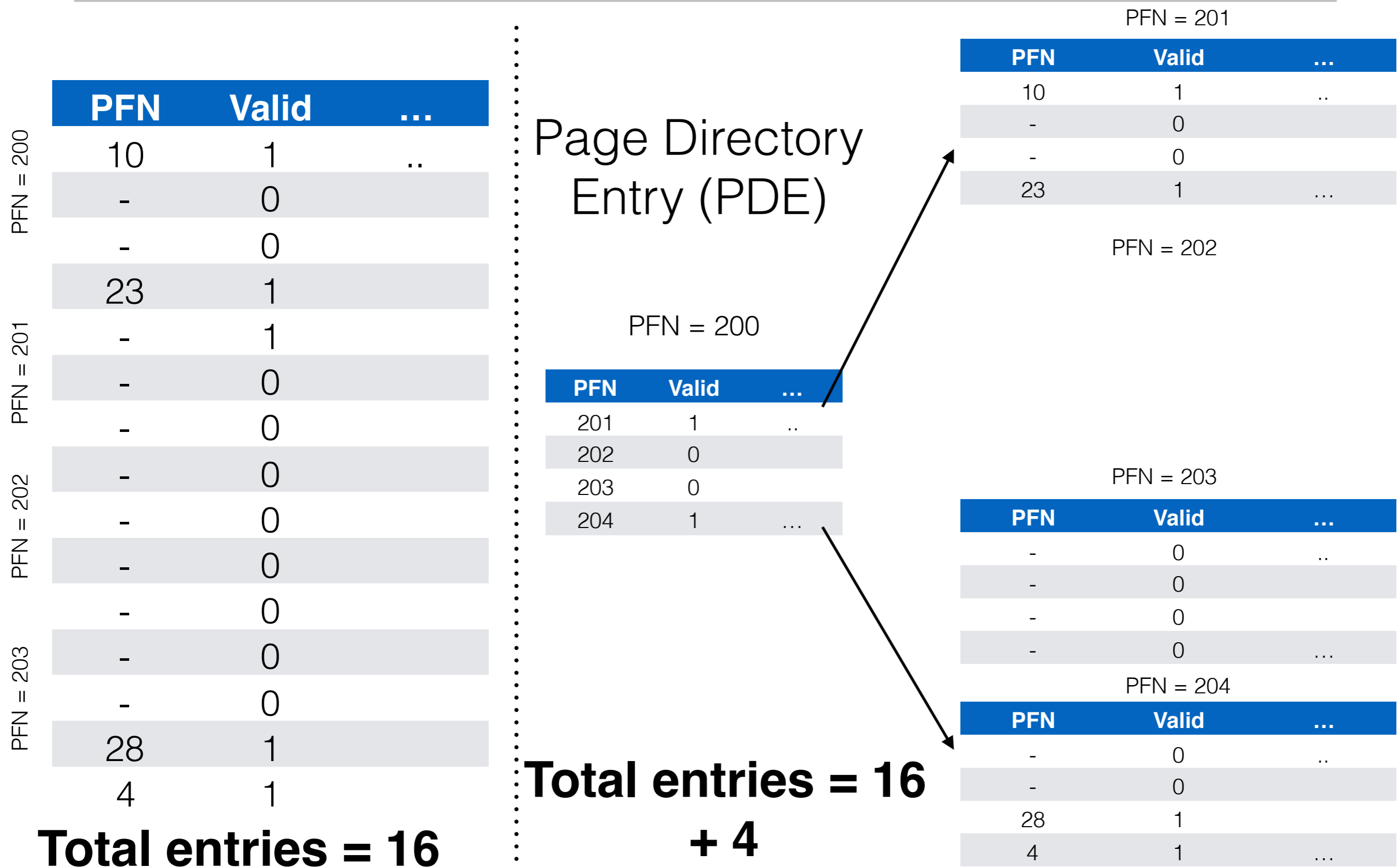
# Reducing Memory Overheads of Paging - Segmentation + PT



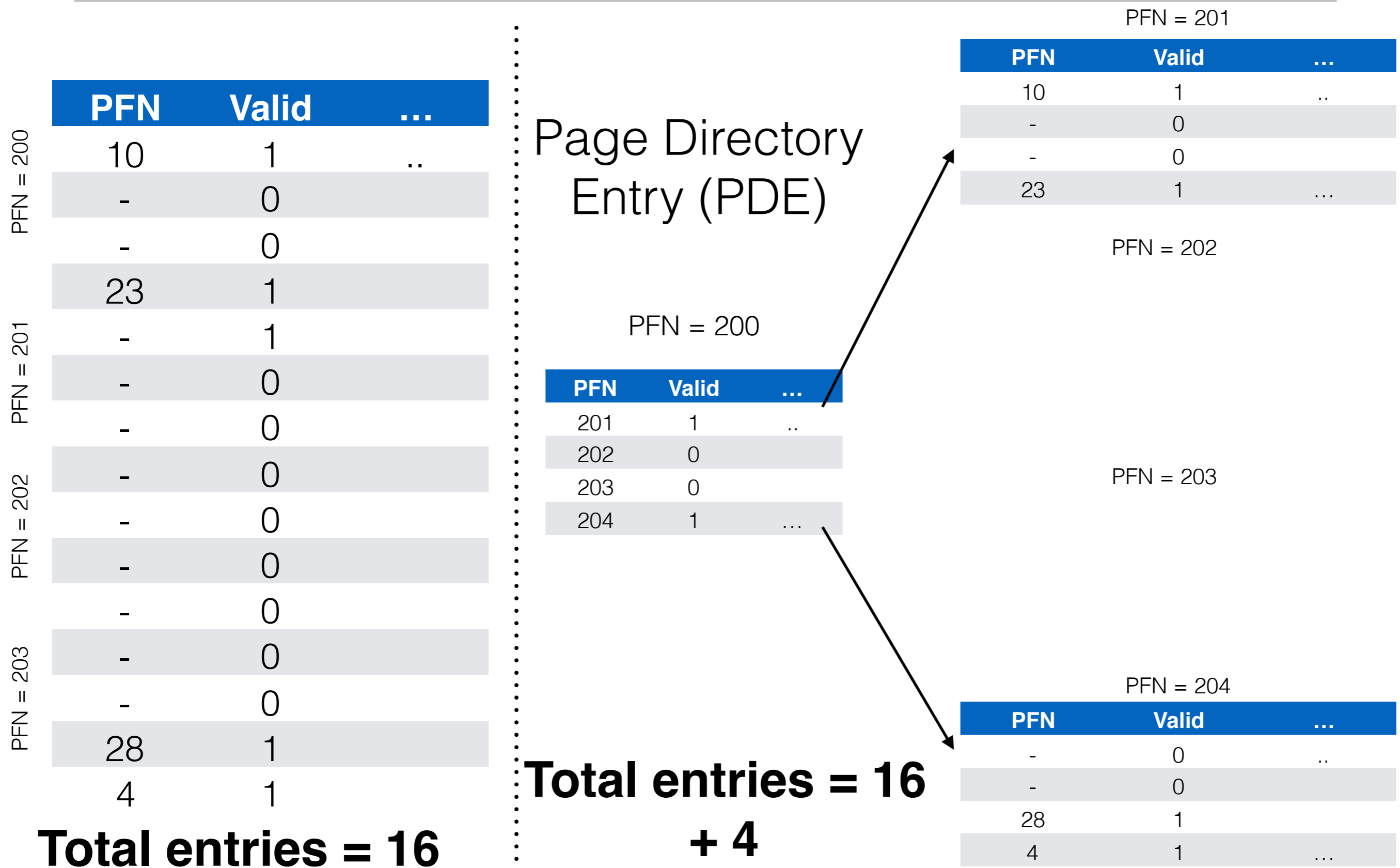
# Reducing Memory Overheads of Paging - Segmentation + PT



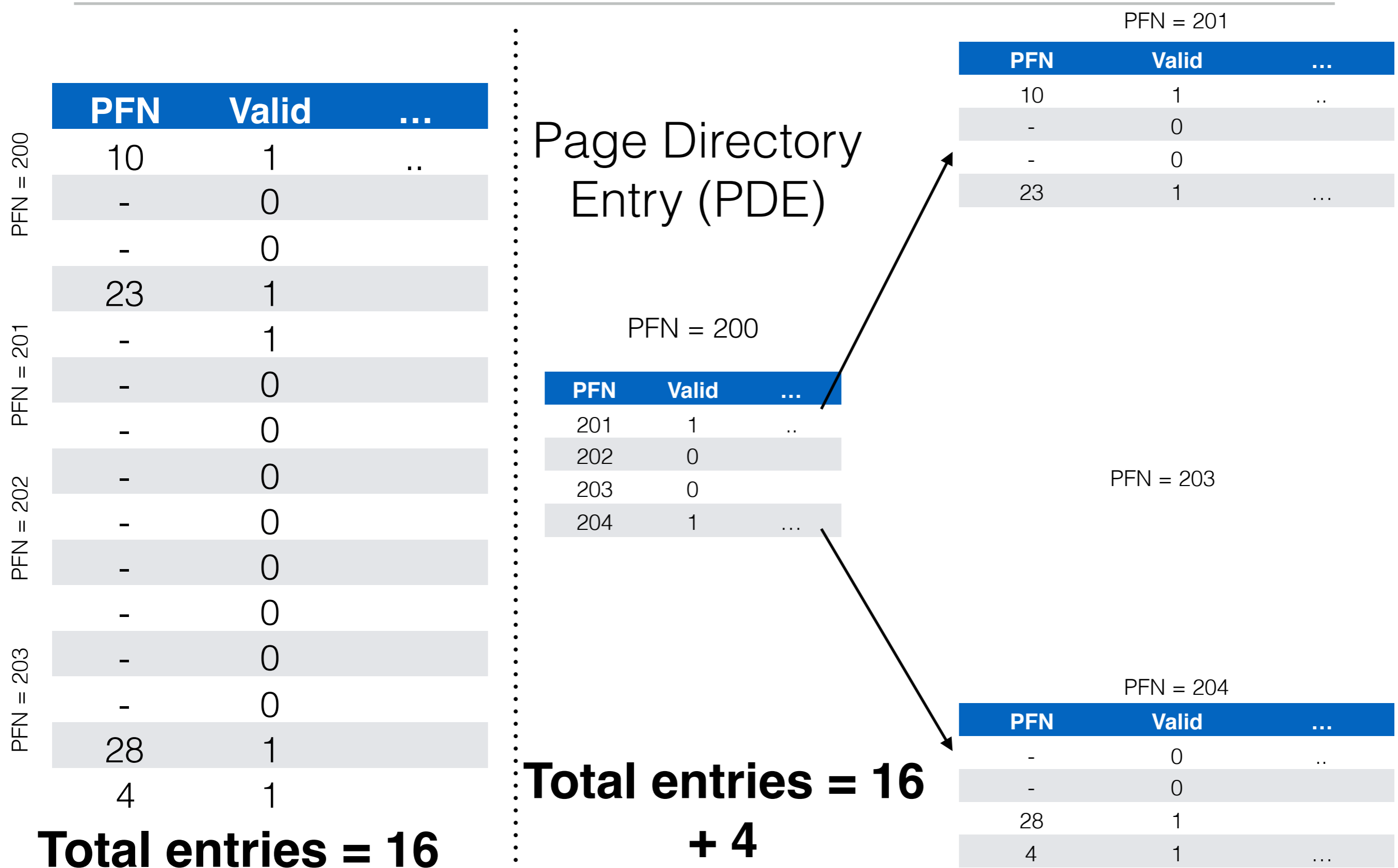
# Reducing Memory Overheads of Paging - Segmentation + PT



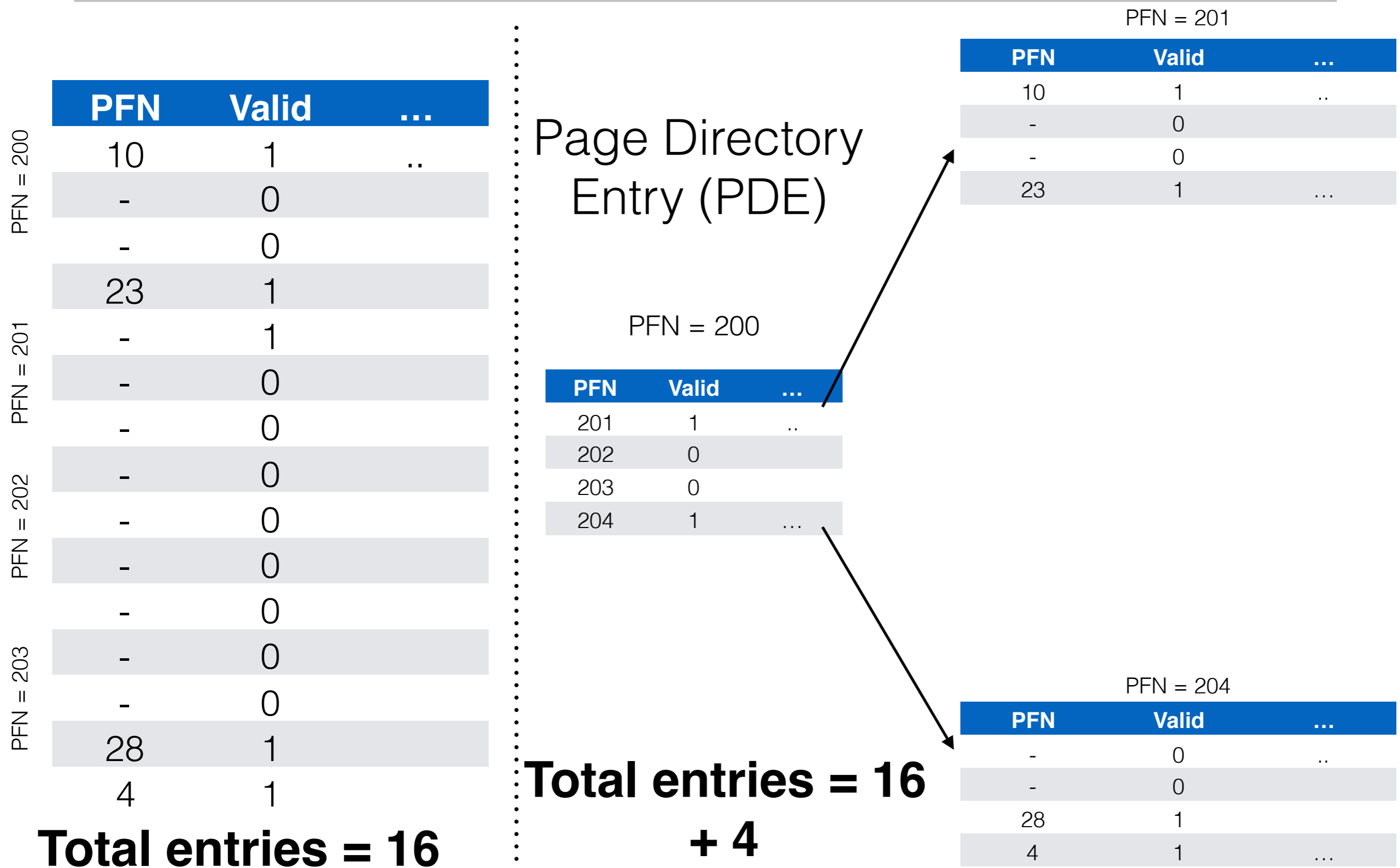
# Reducing Memory Overheads of Paging - Segmentation + PT



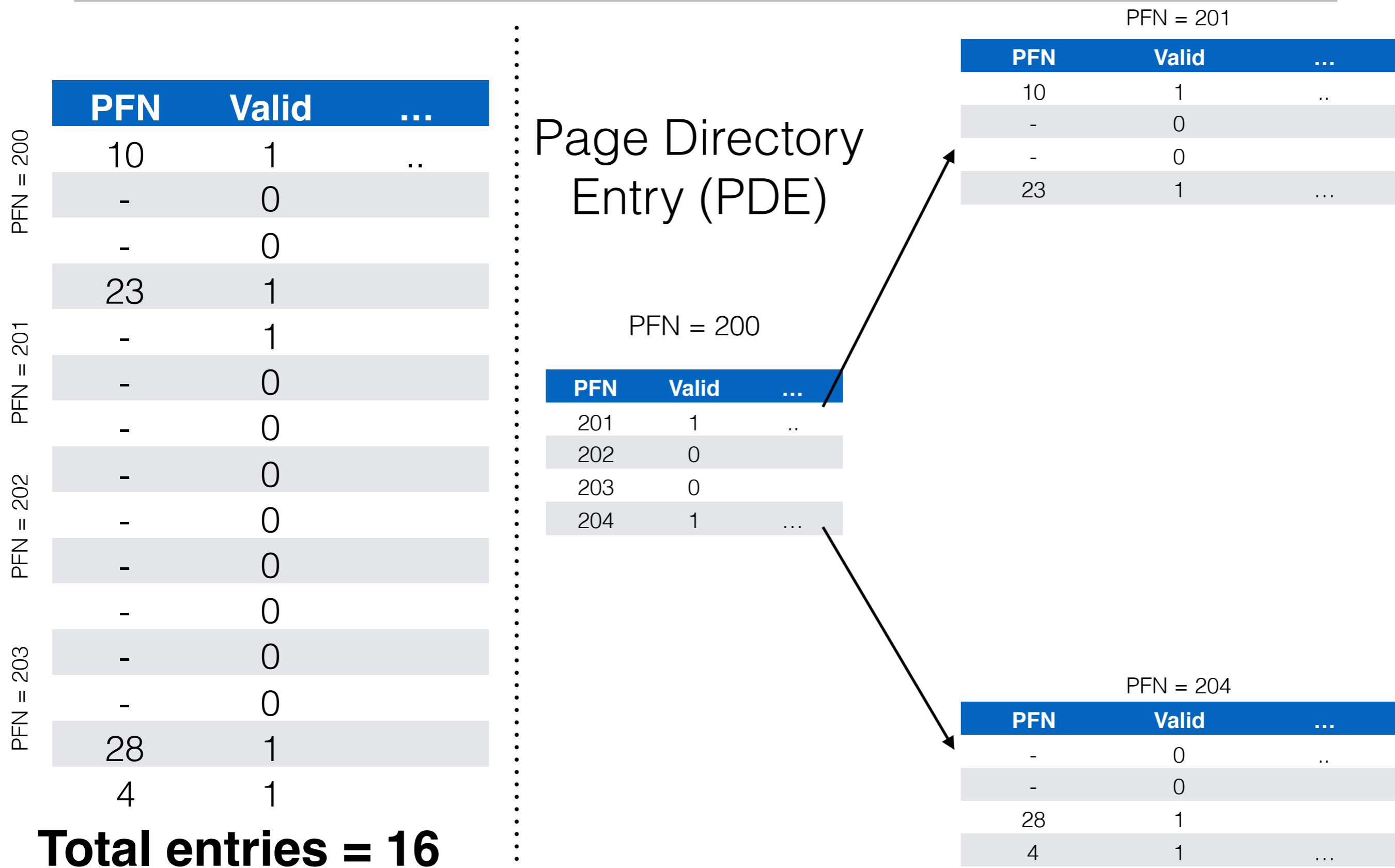
# Reducing Memory Overheads of Paging - Segmentation + PT



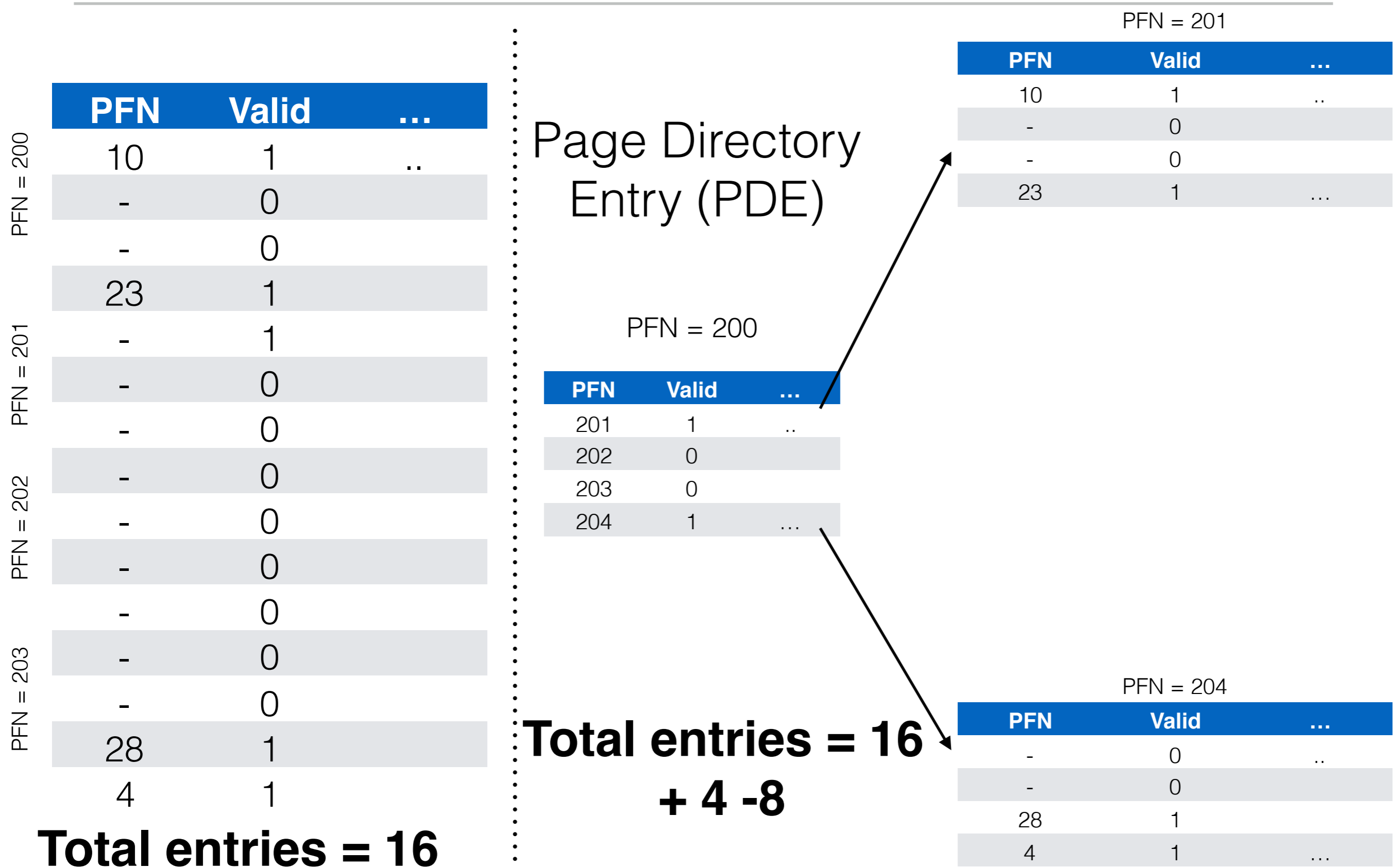
# Reducing Memory Overheads of Paging - Segmentation + PT



# Reducing Memory Overheads of Paging - Segmentation + PT



# Reducing Memory Overheads of Paging - Segmentation + PT





# Reducing Memory Overheads of Paging - PT + PT (Multi-level Paging)

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# Reducing Memory Overheads of Paging - PT + PT (Multi-level Paging)

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- Multi-level paging allocates memory proportional to requirement

# Reducing Memory Overheads of Paging - PT + PT (Multi-level Paging)

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- Multi-level paging allocates memory proportional to requirement
  - Sparse address spaces well supported

# Reducing Memory Overheads of Paging - PT + PT (Multi-level Paging)

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- Multi-level paging allocates memory proportional to requirement
  - Sparse address spaces well supported
- Previously, we needed 4 MB contiguous space for PT memory

# Reducing Memory Overheads of Paging - PT + PT (Multi-level Paging)

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- Multi-level paging allocates memory proportional to requirement
  - Sparse address spaces well supported
- Previously, we needed 4 MB contiguous space for PT memory
  - Now?

# Reducing Memory Overheads of Paging - PT + PT (Multi-level Paging)

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- Multi-level paging allocates memory proportional to requirement
  - Sparse address spaces well supported
- Previously, we needed 4 MB contiguous space for PT memory
  - Now?
    - Can place Page Tables anywhere in memory with multi-level paging...