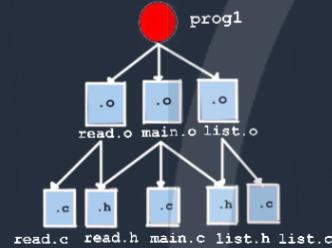


# Advantages

- Makefiles can be a lot handier in large software projects, as using Makefiles can substantially reduce build times if only a few source files have changed, and help automate the process.

- Automation
- Simplicity
- Almost no dependencies

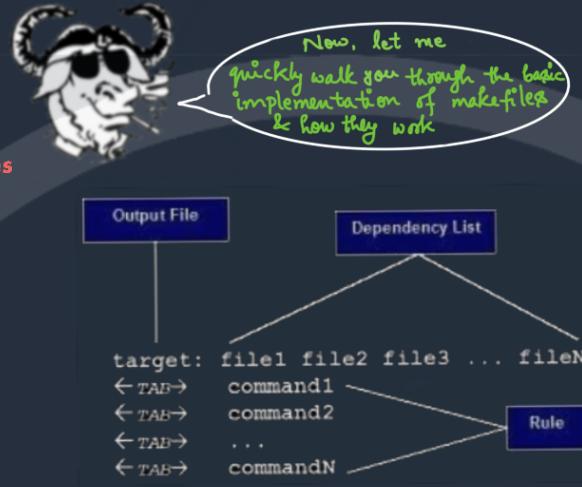
 Not Makefiles use a dependency graph. If none of the files that are prerequisites have been changed since the last time the program was compiled, no actions take place.



 If only one file is modified, will it compile all the files all over again?

- The makefile is recursively carried out (with dependency prepared before each target depending upon them) until everything has been updated (that requires updating) and the primary/ultimate target is complete
- These instructions with their dependencies are specified in a makefile.

 Yes! That is the case indeed. In makefile we can define the exact order in which we want our rules / commands to execute.



**Defining Variable**

```
BFLAGS = -f filelist.txt
TARGET = riscv_output
help:
@echo make sort      build and run all sort hex files
@echo make xor      build and run all xor hex files
sort:
cd .../mem_generator && $(MAKE) clean
$(MAKE) sort -C ..../mem_generator
iverilog $(BFLAGS) -o riscv_output
vvp riscv_output
make clean

xor: ← target
cd .../mem_generator && $(MAKE) clean
$(MAKE) xor -C ..../mem_generator
iverilog $(BFLAGS) -o riscv_output
vvp riscv_output
make clean

clean:
@$(RM) $(TARGET)
```

**Sequential compilation & execution of commands / rules**

**Executing System Commands**

- Target: Action to be executed by the rule
- Dependencies: Needed to exist to satisfy the target
- Commands: Sequence of commands to be executed

 Thank you, Benzel! Now I will be able to compile & execute programs more efficiently with this handy automation tool. Enlightenment achieved!

## Approach to Build Automation

 I'm tired of compiling & executing multiple dependent files whenever I change little bit of code.

 Haven't you heard of makefiles? I always use them to automate my files sequentially. A makefile is a file containing a set of directives used by a make build automation tool to generate a target/ goal.

 But I have a lot of dependent files, to be executed in a specific order & spread around different directories. Can makefiles do that?

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Material References

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- <http://www.emblastic.com/blog/06/what-does-a-makefile-contain>
- [https://upload.wikimedia.org/wikipedia/en/thumb/2/22/Heckert\\_GNU\\_white.svg/1200px-Heckert\\_GNU\\_white.svg.png](https://upload.wikimedia.org/wikipedia/en/thumb/2/22/Heckert_GNU_white.svg/1200px-Heckert_GNU_white.svg.png)
- <https://www.toptal.com/c-plus-plus/c-plus-plus-understanding-compilation>